Rugged Mobile Computer



Operators Manual

Chameleon: 3195330, 3195314, 3195316, 3258811
Iguana: 3195329, 3258802, 3258812
Gecko: 3258801
Digital Interface Unit: 3195333, 3195311

Revision Control:
Version 02: 31 October 2000

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Rugged Mobile Computer (RMC)
Operators Manual
Raytheon Company

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Overview

- Please read these instructions thoroughly. Follow the steps below to get started quickly.
- Insert the battery pack into the battery compartment. When the battery is fully inserted into the computer, the computer will begin to boot.
- Connect the AC Power Adapter to line power. The battery pack will begin to charge. If the power adapter is connected to the computer prior to insertion of the battery pack, the computer will begin to boot and the battery/power icon will ***not*** be displayed in the Windows® task bar until a subsequent boot sequence has been completed.
- Configure Microsoft Windows. The unique drivers required for the advanced components and Mil-Std-1553 card, if installed, have been configured at the factory.
- Make backup diskettes.
- Use the Windows shutdown command contained on the Start button for normal system shutdown.
- After the system has been shutdown and with the battery installed, the red on/off button on the right corner of the keyboard can be used to power up the system. This is a momentary switch that applies power as soon as it is pressed.
- To wake the system up from the standby mode, press the red on/off button for approximately one second. In the event the operating system can not be used for a normal shut down, select and hold the red on/off button until the system power LED is extinguished (approximately 5 to 10 seconds).

The hard disk is already formatted and loaded with the MS Windows operating system.

CAUTION
DO NOT FORMAT THE HARD DISK!

Battery and Chargers

A Lithium coin cell battery is used to backup the CMOS memory. This is a UL listed battery. Return the RMC to your service representative for CMOS battery replacement.

CAUTION
Danger of explosion if battery is incorrectly replaced.
Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacture's instructions.

The RMC uses an ACPI compliant, Smart Power Subsystem. This consists of an ACPI compliant Battery pack (96214 ASSY 3195302) and AC Power Adapter (96214 ASSY 3195306). They are the only authorized components for this system. Use of any other components may cause damage to the unit, and injury to the operator.

Because the battery pack is Lithium Ion, special charging requirements are necessary to promote battery life. This is handled automatically by the onboard electronics. From the user perspective, the battery won't necessarily charge, even though the battery has been discharging. What's happening is the onboard electronics are forcing the battery to discharge to approximately 70% capacity. Once it reaches 70% capacity, charging will be initialized until the battery is fully charged. This ensures maximum life for the battery.

Over discharging is another function that is handled by the onboard electronics. If the battery pack reaches a certain level, the battery electronics will shut down automatically, protecting the pack from damage. To prevent the automatic battery shut down from occurring during system startup on battery power, the Power Supply/Charger continuously monitors the battery status. If the battery pack gets below approximately 15% capacity, the system will not power up. The Battery LED will indicate either yellow or solid red depending on the battery state. Simply insert the DC power plug from the power brick, and the unit will power up and begin charging the battery.

Docking

Hot docking is not supported on this platform. While it is electrically safe to physically dock or undock the Chameleon or Gecko unit while power is on, the operating system will not be able to recognize the change in configuration until after a reboot cycle. Therefore cold docking (physically docking or undocking with both the Chameleon or Gecko and the Digital Interface Unit (DIU) powered off) is recommended. When docked to the DIU, the system (DIU) must be powered with AC power. Battery powered operation while docked to the DIU is not supported.

Video Setup

Acceptable flat panel display resolutions:

- Color palette: 16, 256, High Color (16-bit), or True Color (24-bit)
- Desktop area: 640 x 480 (VGA), 800 x 600 (SVGA) or 1024 x 768 (XGA)

Recommended display resolution is set at the factory.
Note that higher video resolutions are possible when using an external monitor and with the flat panel display disabled.

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WARNING

The computers are shipped with the recommended video setting for the flat panel provided with the computer.

DO NOT CHANGE THE MONITOR RESOLUTION SETTING!

Rugged System Usage

The RMC offers leading edge modular technology in a state of the art, rugged form factor. The computer has the processing power of a desktop, but the portability of a notebook. The RMC features the Pentium® II processor. Its packaging lends itself to be sunlight readable, operate in extended temperature ranges and in elevated shock and vibration environments. The materials and packaging have been selected to resist corrosion and fungal growth. The unit has been tested through extended Highly Accelerated Life Tests (HALT) and also unique environmental tests. The case, mouse and keyboard have been sealed for resistance to rain and moisture. MIL-STD-810 was used as a guide verification testing. These features, along with the modular system architecture, allow the system to be configured to meet your needs.

CAUTION: When opening access doors and connecting power in certain environments, good judgment should be used to avoid internal system damage. There is no environmental seal provided when a door has been opened.

System Description

The RMC has the following components:

- 233MHz Intel™ Mobile Pentium II Processor in an MMC-2 Cartridge.
  or
  266 MHz Intel™ Mobile Pentium II Processor in an MMC-2 Cartridge.
  or
  333 MHz Intel™ Mobile Pentium II Processor in an MMC-2 Cartridge.
    - 82443BX (North Bridge) Host Bridge system controller.
    - 512KB L2 Cache.
- Flat panel display.
- 64 MB DRAM in one SODIMM sockets (baseline system).
- 60GB or greater IDE Hard Disk Drive (baseline system).
- 24X CDROM.
- 3.5” 1.44MB Floppy Disk Drive.
- Phoenix 4.06 BIOS in a 28F400B5T Flash Boot Device (512KB).
- Chips & Technology 69000 High Performance Flat Panel / CRT HiQVideo Accelerator with Integrated Memory (2MB).
- Two Texas Instruments TI PCI1251B Card Bus controllers providing four CardBus slots compatible with type I, II, and III PC Cards.
- Zoomed Video Port input from the external CardBus controller (available to either slot) that allows accelerated video and audio input and playback.
- Intel 82558 Fast Ethernet PCI Bus Controller with integrated PHY 10/100 BaseT.

- Single USB port using a optional multimedia cable. Legacy USB is supported in the BIOS to provide keyboard and mouse support. This allows BIOS setup to be controlled via a USB keyboard.
- SymBIOS SYM53C860 SCSI Controller
- One Bi-directional parallel port.
- Two serial ports. One RS-232 and another with RS-485/RS-422 protocols.
- SoundBlaster Pro compatible Crystal Audio Device (CS 4237 B).
- External PS/2 port. There is one 6-pin PS/2 mini-DIN connector that can be split out to facilitate simultaneous use of an external keyboard and mouse.

The following components exist on the Docking Interface Unit (DIU):

- Intel 82380FB/AB Dock set providing PCI-PCI bridge as well as PCI-ISA bridge.
- SymBIOS 53C875 SCSI Controller
- Two PCI Slots.
- Two ISA Slots.

Definition of Terms used in this document

ACPI	*Advanced Configuration and Power Interface*. A key element in the move toward Operating System Directed Power Management (OSPM). ACPI incorporates the functionality of APM1.2 and the Plug and Play BIOS.
AGP	*Accelerated Graphics Port*. A separate bus between the graphics controller and 440 BX chipset. This high speed bus is designed for 3D graphics and digital video applications.
APM 1.2	*Advanced Power Management Version 1.2*. A connection-oriented software interface specification that allows operating system device drivers to control the power management functionality of a PC.
BDA	*BIOS Data Area*. A 256 byte block of DRAM starting at address 400h that contains data initialized and used by the System BIOS detailing the system configuration and errors encountered.
BIOS	*Basic Input and Output Services*
BIOS Extension	An object code module that is typically integrated into the FBD or placed into a ROM that is accessible on the peripheral bus (PCI, ISA, etc.) in the address range 0C0000h through 0DFFFFH.
CSR	*CMOS Save and Restore*. A System BIOS feature that allows the user to backup the contents of CMOS RAM (contained within the real time clock) to the BIOS Flash device to be restored later if necessary (such as when the real time clock battery fails).
ECP	*Extended Capabilities Port*. An enhancement of the standard PC parallel port that allows high speed bi-directional data transfers and other features.
ESCD	*Extended System Configuration Data*. A block of nonvolatile memory that stores information on the devices found and configured by the Plug and Play BIOS.
FBD	*Flash Boot Device*. The boot block flash device used to store the System BIOS and possibly other firmware modules. The code in this device is the first code executed when a PC boots.
LBA	*Logical Block Addressing*. A newer means of addressing data on a hard disk. Standard PC hard disks use Cylinder/Head/Sector (CHS) addressing where each of these parameters are specified by the hard disk driver when it reads or writes to the disk. LBA allows the driver to address logical blocks on the disk (cylinder 0, head 0, sector 1 = logical block 0). This mechanism is simpler and typically more efficient, but requires that the System BIOS and operating system understand how to deal with LBA hard disks.
NMI	*Non-maskable Interrupt*.

POST	*Power On Self Test.* The hardware tests and initialization that the System BIOS performs when the PC is booting.
RMC	Rugged Mobile Computer
RTC	*Real Time Clock.* The standard Motorola 146818A-compatible real time clock used in PC-ATs. This device also contains 114 bytes of CMOS RAM whose contents are maintained by an external battery.
SCI	*System Control Interrupt.* This interrupt is asserted by the system to inform the ACPI aware operating system of ACPI events such as thermal events, lid events, power button events, etc.
SCSI	*Small Computer System Interface.*
SDRAM	*Synchronous Dynamic Random Access Memory.*
SMI	*System Management Interrupt.*
SMM	*System Management Mode.*
SPD	*Serial Presence Detect* is a technology that allows the BIOS and operating system to query the system memory to determine required parameters for memory configuration.
UBE	*User BIOS Extension.* A BIOS extension that is stored in the FBD and mapped into ISA bus memory and scanned at boot time. The mapping and execution of a UBE is under the control of CMOS setup.
UMB	*Upper Memory Block.* A block of memory reserved for device drivers in order to free up conventional memory.
USB	*Universal Serial Bus.* A new serial data bus that is intended to eliminate the need for separate serial, parallel, mouse, keyboard, joystick, etc. ports on a PC-compatible.

System Setup

Unpacking

The RMC and DIU are supplied in a custom-built transit case, which protects the assemblies until they are ready to use. Inside the transit cases are foam inserts, which have been cut to accept and protect the units and their accessories. Unpacking is straightforward. The units are supplied with the desired operating system loaded and ready to operate. Power input can be external universal input or the battery may be used. Battery level should be checked upon receipt to see if charging is required.

Initial Startup

The RMC is shipped ready to use. The computer will boot up when the battery is installed. If universal power is used, the computer will boot up when the AC Adapter is connected. Once either the battery is installed or the system is connected to AC power using the Adapter, subsequent initiation of the boot up cycle can be accomplished by pressing the On/Off switch.

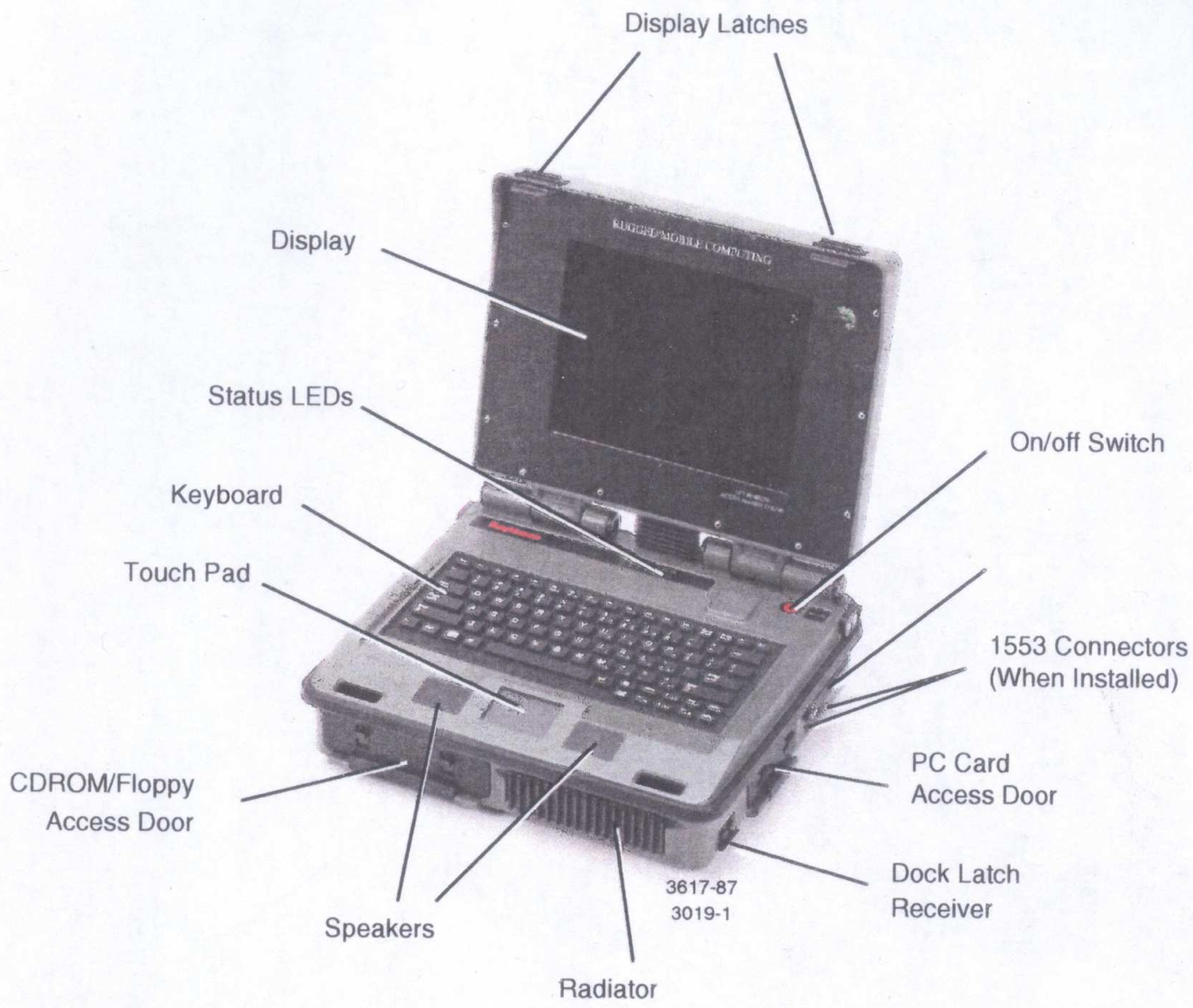
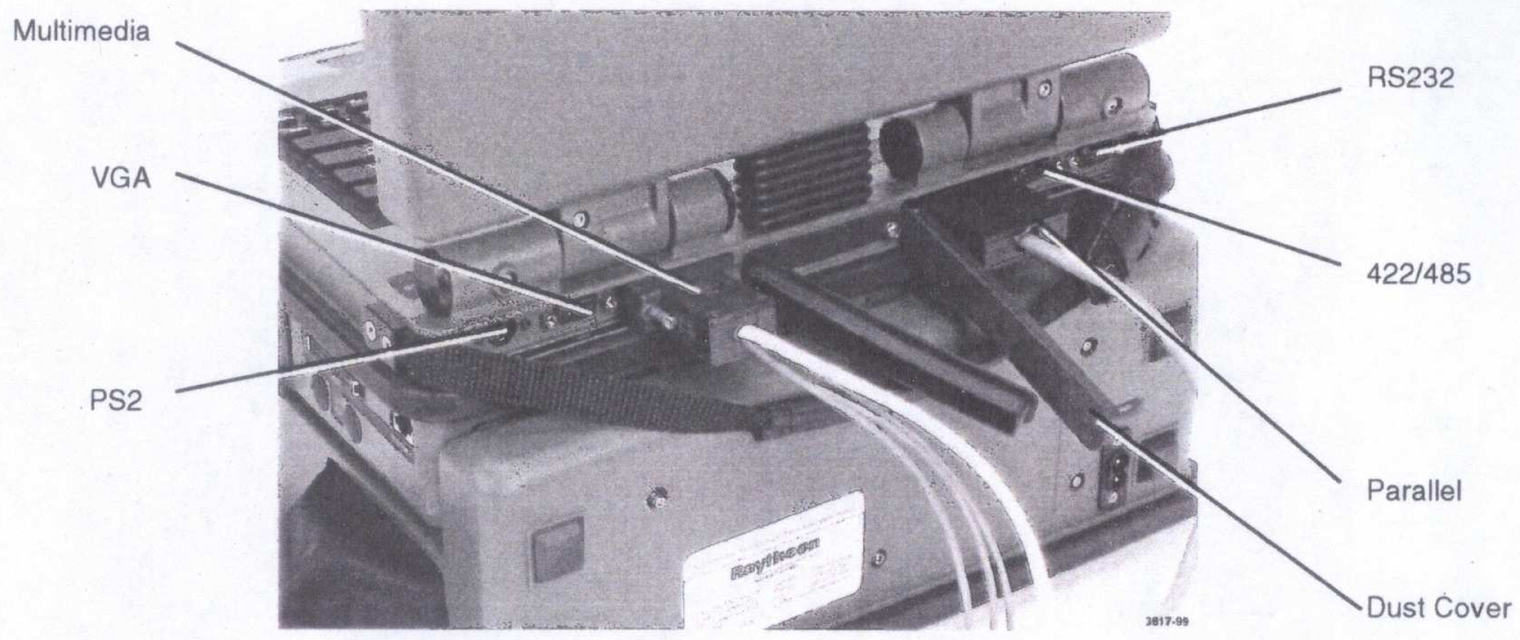


Figure 1 - Front Isometric View (Chameleon shown)

Note: Display and display latches are Chameleon and Iguana RMC's only.





3019-2

Figure 2 - Rear Isometric View

Display

Care should be taken not to scratch the display. Under harsh lighting conditions it may be necessary to reposition the unit to increase the readability of the display.

Details

The RMC uses the Chips and Technologies 69000 HiQVideo Controller. The C&T 69000 is functionally equivalent to the C&T 65555 but includes 2MB of video SDRAM on-chip.

The C&T 69000 GUI-Accelerated SVGA/XGA controller chip on the CPU board provides video support. The VGA controller sits on the PCIbus and controls both a SVGA/XGA monitor connected to the VGA connector and a Color flat panel display.

The 69000 comes integrated with 2MB of high performance SDRAM onboard the video controller. This eliminates the need for any external video memory.

The controller will support the following video resolutions on the CRT under Windows 95/98/NT. The CRT modes are limited to the resolution of the Flat Panel if simultaneous LCD/VGA is enabled.

Table 1. CRT Video Resolutions

Screen Format (Pixels)	No. of Colors	Refresh Rates	Memory Required
640x480	256	60, 75, 85	300KB
640x480	65,535	60, 75, 85	600KB
640x480	16.8 Million	60, 75, 85	900KB
800x600	65,535	60, 75, 85	938KB
800x600	16.8 Million	60, 75, 85	1.37MB
1024x768	256	60, 75, 85	786KB
1024x768	65,535	60, 75, 85	1.50MB
1280x1024	256	60	1.25MB

Note that 1024x768 with more than 64K colors and 1280x1024 with more than 256 colors requires a frame buffer larger than 2MB.

A Zoom Video (ZV-Port) interface from the external CardBus controller is available to the 69000 controller. A CardBus card can route digital video information directly to the VGA frame buffer in either RGB or YUV format. A combination of drivers for the CardBus card and the 69000 enables this interface.

Flat Panel Backlight Control

Backlight luminance (brightness) control is provided by a 31-step digital POT controlled by hotkeys on the keyboard. If the hotkey is set up to auto-repeat, the full range of brightness can be traversed in 31 steps/10 key-per-sec = 3.1 seconds. The digital POT is non-volatile, which means it will store its state through power cycles.

Status LEDs

The LED functions are listed here in the order that they appear on the top of the keyboard assembly, from left to right:

Table 2. Status LEDs

BATT	This bi-color LED indicates the status: LED — Status **Off** — System off, battery low, not charging **Green** — System on, battery ok **Amber** — System on, battery charging or System off, battery low and charging **Red** — System on, battery low and charging NOTE: If you attempt to turn the system on with a low battery (below approximately 15% capacity), a red LED will be shown and the unit will not power up. To resume normal operation, the unit must be powered by the AC Adapter or a spare battery must be installed. Once AC power is applied the battery should begin the charging cycle. Once the battery is recharged, battery powered operation can be resumed.
PWR	This Bi-color LED indicates the status of the system: **Green** indicates that the system is running **Off** indicates that the system is in the Soft-Off or Mechanical Off state **Amber** indicates that the system is in a sleep state
IDE	This **Green** LED indicates hard disk drive activity on either the primary or secondary IDE port (i.e., CDROM or Hard Disk Drive).
FDD	This **Green** LED indicates the Floppy drive activity.
CAP	This **Green** LED indicates the state of the Cap Lock.
NUM	This **Green** LED indicates the state of the Num Lock.
SCRL	This **Green** LED indicates the state of the Scrl Lock.

Keyboard

Details

The keyboard controller supports two external PS/2 devices. One mouse and one keyboard are supported on the External ports (not two mice or two keyboards) and powered at 5V. External devices may be hot-plugged.

The Audio hot-key state is lost when power is removed from the system. However, it is expected that the OS drivers for the audio device will save the context of the audio IC before power-down. Note that the original volume settings will not be re-initialized on the next power-up cycle until sometime in the OS boot process. Therefore, sounds such as PC-speaker "beeps" are heard as the system boots regardless of the non-volatile state.

The LCD Brightness state is non-volatile, saved in a digital POT on the board.

PC Card Access

Details

Two Texas Instruments PCI1251B PCI to CardBus Host Adapter chips supply two CardBus and PC Card interfaces. One CardBus socket set is for internal cards and one is available for operator usage. The PCI1251B is PCI 2.1, PC Card Standard, and ACPI 1.0 compliant.

The PCI1251B CardBus controllers are connected to IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15 and PCI INTC. Interrupts from 16-bit PC-Cards (PCMCIA cards) use the legacy IRQ signals and 32-bit PC-Cards (CardBus cards) use the PCI INTC interrupt. The PCI1251B Card Status Change circuitry may also use the PCI INTC signal, depending on the driver.

PCMCIA card DMA cycles are also supported.

The Internal PC-Card slots support one or two type I or II PC-Cards or one type II and one type III. The external PC-Card slot supports one or two type I or II PC-Cards, or one type III PC-Card.

The power to the PC-Card slots is 0V, 3.3V or 5V for VCC and 0V, VCC or 12V for VPP. The VPP1 and VPP2 pins are connected together, thus providing only one programming voltage. In order to conserve power, the internal CardBus slots do not support the 12V programming voltage.

Zoom Video and Zoom Audio ports are supported by the External CardBus controller only, allowing CardBus cards to stream digital data directly into the video frame buffer and/or the audio circuit.

Card Installation

PCMCIA or PC cards are installed in their respective slots simply by sliding in the cards until seated. The cards need to be pressed firmly to insure that the pins are fully engaged. Cards are removed by pressing the release buttons located on the left side of the card facing the slot. These buttons, when pressed, will release and eject the card from the connector pins.

IDE Hard Disk

The physical size of the HDD is critical to insure that the drive is properly shock isolated. Only use the Raytheon supplied HDD.

Removing HDD

The HDD is removed and installed through the access cover in located in the battery cavity. The computer must be removed from the dock to gain access. Drive replacement is best accomplished with the computer display assembly closed and the computer on a flat surface resting on the closed display housing.

Caution: To avoid possible damage to the computer and its components the computer needs to be in the off position before changing the HDD. Care should be taken not to touch the exposed pins on the HDD and ESD practices should be used, if possible.

The access door is opened with one screw using a small flat blade screwdriver. The HDD is supported with foam on all sides including foam from the HDD door. As the door is opened tension will be felt from the door gaskets. With the door fully opened and resting in the open position the HDD can be lifted out of the cavity using the attached pull tang.

Caution: When removing the HDD be careful not to damage the flex circuit or connector pins.

Remove the connector by firmly holding the HDD and pulling the connector shell and flex off the connector. Note the orientation of the connector.

Installation of a new or alternate HDD is accomplished in the reverse manner.

Details

The Bus Master Enhanced IDE Interface supports Modes 1, 2, 3, 4 as well as Bus Master (DMA) modes 0, 1, and 2 and Ultra DMA/33. The obsolete IDE register at I/O address 3F7h is not supported.

There are two separate IDE channels (Primary and Secondary) with capabilities for Master and Slave on each of the channels. However, to improve interrupt availability, only the Primary channel is used for the internal IDE HDD and CDROM drive, allowing the Secondary channel to be disabled in the BIOS.

Floppy & CDROM Access

The access doors for the Floppy & CDROM assembly have a compression seal using a O-ring. The door is opened and closed by pushing firmly on the two latches. This will slightly compress the O-ring and allow the latches to move to the open position. The door will open freely. Upon release of pressure off the latches they will return to the closed position.

To close the door, reverse the above procedure.

Note: There are arrows on the outside of the door, which indicate the direction which will open the latches. A red indicator can be seen if the latched are in the open position.

Floppy Disk Controller

The National Semiconductor PC87309 is used to implement a standard PC floppy disk port. The device resides on the ISA bus, and is accessed at the standard PC I/O addresses of 3F0h-3F7h. Although other interrupts and DMA channels can be used, IRQ6 and DMA2 are used to maintain PC compatibility. Only one floppy disk drive is supported.

An LED on the IO board will notify the user of floppy disk drive activity. The LED is lit when the Drive Select signal to the floppy is active.

Thermal Radiator

Even though the RMC has internal thermal management, the computer has a Thermal Radiator located on the front, next to the CD/Floppy door to help the processor run at its maximum performance. The temperature of the radiator will vary depending on processor demand.

Speakers

There are two speakers located under pads on each side of the mouse pad. The speaker volume can be adjusted using the function keys on the keyboard or through the operating system. If additional volume is needed and conditions are acceptable the CD/Floppy door can be left open. For amplified sound, the optional multimedia cable can be used in conjunction with powered external speakers and or sound system.

Mouse

The RMC has a touch pad for mouse commands. The touch pad is located just below the keyboard between the speaker ports. For a mouse click simply tap on the pad. Tap twice for a double click. Tap and hold to drag, draw or highlight a selection. Drag to the edge of the pad and dragging continues until your finger is lifted. For right click mouse functionality, tap the upper rignt corner of the mouse. Touch pad setup is available by opening the Window Control Panel and clicking on the mouse icon.

External Ports

SCSI

The RMC system includes two SCSI-3 controllers: one in the computer, and one in the DIU. These two controllers operate independently.

The external SCSI port on the RMC is accessed by removing the SCSI/ENET door on the right side of the computer.

A Symbios 53C860 is used to implement the CPU board 8-bit Ultra-SCSI-3 controller. The 53C860 is a 32-bit PCI device that resides on the primary PCI bus, and provides a PCI-to-SCSI interface. The RMC supports single-ended SCSI connections, which allow Ultra SCSI synchronous transfer rates up to 20MB/s, Fast SCSI synchronous transfer rates up to 10MB/s, and asynchronous transfer rates up to 7MB/s. The signals on the SCSI connector include ESD protection.

The CPU board SCSI controller may be enabled or disabled under BIOS control.

The RMC SCSI implementation includes programmable termination for the SCSI bus. The on-board SCSI termination is enabled or disabled via CMOS setup. In addition, the active SCSI terminators can set to a low-power mode where they only terminate with 1ma drivers. This can be used in configurations with cables less than 1 foot.

A Symbios SYM53C875 is used to implement the 16-but Wide Ultra-SCSI-3 controller in the Digital Interface Unit. The 53C875 is a 32-bit PCI device that resides on the secondary/dock PCI bus, and provides a single-chip PCI-to-SCSI interface. It supports single-ended Wide Ultra-SCSI synchronous transfer rates up to 40MB/s, Fast SCSI synchronous transfer rates up to 10MB/s , and asynchronous transfer rates up to 7MB/s.

The DIU board SCSI controller may be enabled or disabled under BIOS/ACPI control. At reset the SCSI controller is enabled.

Ethernet

10/100Mbps Ethernet Interface

An Intel 82558 Ethernet controller is used on the Chameleon to implement a high performance PCI-based 10/100Base-T Ethernet interface, available on a RJ-45 connector on the right side of the computer next to the SCSI port. Network booting is not supported.

The Ethernet controller may be enabled or disabled in CMOS setup.

The following ports are accessed by removing the dust cover . Locations are shown in figure (3019-2)

PS/2

There is a PS/2 six pin mini-din for connection of an external keyboard, bar code scanner, or mouse.

External Video

The RMC has an external VGA DB-15 female connector for connection to an external monitor.

Multimedia

Audio Interface

The multimedia connector allows external connection for a mono microphone, line in and line out, as well as a USB interface port. This connector does not follow any industry standards and as such requires the optional Multimedia cable. Contact the Technical Support office and reference Part number Raytheon Part Number 3195295-8.

USB Interface

The RMC supports the Universal Serial Bus (USB), a peripheral interconnect bus for many devices including keyboards, mice, joysticks and many other devices. The USB Controller use 16 I/O registers that are located in I/O space by the BIOS configuration. In addition, the USB controller uses PCI interrupt ~PIRQD, which controlling software will map to a free ISAbus interrupt. The USB implementation does not support USB over-current detection.

The RMC supports only a single USB port. The port connection is on the optional Multimedia cable.

Docking connector

The Docking connector is located on the motherboard and accessed by removing the dock door prior to docking the computer to the Digital Interface Unit station. The dock door should only be removed when docking since removal eliminates the environmental seal. The docking connector is a self-aligning connector using guide pins and sockets. There are also mechanical features that interface and hold the Chameleon or Gecko to the DIU when docked.

Parallel

The IEEE1284 parallel port can be configured to run in standard mode, enhanced mode (EPP) or Microsoft high-speed mode (ECP). MSDOS and Windows will recognize this port as LPT1. The parallel port can be configured to have IO ranges matching PC standard locations for LPT1, LPT2 and LPT3 via CMOS setup. In addition, the parallel port can use any one of IRQ3-7 or IRQ12, and DMA1 or DMA3 in ECP mode.

RS-232 & RS-422/485 Serial Ports

The Serial ports are 16C550 compatible UARTs with send/receive 16-byte FIFOs.

The COMA port will meet the electrical portion of the EIA/TIA-232-E. COMA signals are available on a male DB9 connector at the rear of the unit.

The COMB signals are driven/received by LTC485I RS-485/422 transceiver ICs. The RXD and TXD signals are RS-422 compatible with differential receiver and driver, respectively. Outputs TXD+ and TXD- are tristated if RTS is unasserted for RS-485 multidrop compatibility.

While the RS-422/485 driver will require a 120 ohm termination for proper operation, no terminations are provided on the Chameleon.

Both the COMA and COMB ports can be configured to be at the standard COM1 (3F8h), COM2 (2F8h), COM3 (3E8h) or COM4 (2E8h) addresses, and may use either IRQ4 (COM1 or COM3) or IRQ3 (COM2 or COM4). IRQs can be routed to one of IRQ3-7 or IRQ12.

Display Latches

There are two display latches which are over center type and are used to lock the display down in a closed position (Chameleon and Iguana only).

Dock Receivers

These are used only when docking. Their operation is described in the DIU section if this manual (Chameleon and Gecko only).

CMOS/RTC

A PC/AT compatible real-time Clock (RTC), implemented like a Motorola 146818A including 256 bytes of battery backed CMOS RAM is provided. The RTC circuit uses a 32.768 kHz crystal and generates its own clock.

The backup battery used is a Sony CR2032 20mm 3V lithium battery or a form, fit and function equivalent, with a 200mAh capacity. Replacement of the backup battery should be accomplished by Raytheon Service personnel.

FLASH Boot Device

The BIOS is contained in an Intel TE28F400B5-T80 Smart Voltage Boot-Block FLASH device. The main and parameter blocks of the BIOS may be reprogrammed under program control. Only the boot-block is write protected by a jumper.

The boot block is typically NEVER reprogrammed, even when the main and parameter blocks are reprogrammed. The capability to program the boot block is provided on the Chameleon to facilitate quick changes in manufacturing.

The flash BIOS device is memory addressed and resides in the last 512K of system memory at address FFF80000h to FFFFFFFFh. They are also aliased to the ISAbus real-mode space at F80000h to FFFFFFh.

SoundBlaster Compatible Audio

A 16-bit Sound Blaster Pro™ compatible audio system based on a Crystal Semiconductor CS4237B controller is provided. The audio system will provide for playback of PCM sound data and FM synthesized music as well as audio signals input from various sources, each of which can be mixed under software control. The two independent PCM channels incorporate DMA to reduce processor overhead during play. Internal registers allow adjustment of left and right channels when connected to an external stereo system. Keyboard hot-keys control the master volume and mute functions. The OS drivers can vary the volume of the output under software control via registers within the device.

The input audio sources include the CDROM (Aux-2), External CardBus controller Zoom-Audio (Line-In), an external Line input (Aux-1) and a mono microphone input. Note that the External CardBus Zoom-Audio port may require using the CS4237B controller in a non-Sound Blaster compatible mode due to the large number of audio inputs needed to support these functions.

The monaural speaker port from the processor's chip set and the speaker-out from the two CardBus Controllers are XORed together and routed through the sound controller as well. This PWM audio is added to the audio output at the audio amplifier. Default (power-on) level is set to one-half full volume, and can be adjusted by the application. The PC speaker port is expected to be used as a debugging tool during power-on self-test (POST), but may be used at any time if a suitable driver is installed.

A line-level output is provided directly from the CS4237B controller for external use. This signal is not amplified and is not capable of driving a headphone.

Note that:

- Attaching a device to the line-level output connector may effect the quality of the speaker outputs.
- Plugging a connector into the line-level output will not disable the internal speakers.
- The volume controls work on both the line-level and the speaker outputs simultaneously.

An audio amplifier section provides up to 2 Watts/channel RMS into the internal 8-ohm speakers. The audio amplifier is AC coupled to the speakers to prevent high DC currents from overloading the amplifier. The speaker output is simply an amplified version of the line-level output.

Docking Interface Unit

Docking General Information

The docking interface will not support port replication of any ports on the CPU board. All I/O ports on the CPU board are functional and physically accessible when the system is docked.

Only Type I docking is supported – that is, docking where the DIU board and the CPU system have their own independent power sources. (Type II docks take their power from the CPU system).

The sequences of events to perform the joining of the PCI buses across the dock are handled completely by hardware state machines. This allows hot docking and undocking to occur from the hardware perspective. However, additional software support for enumerating and configuring the newly connected (or disconnected-connected) buss would be required for hot and warm docking.

The Chameleon/Gecko does not support hot docking. While it is electrically safe to physically dock or undock the unit while power is on, the operating system will not be able to recognize the change in configuration until after a reboot cycle. Therefore cold docking (physically docking or undocking with both the Chameleon/Gecko and the DIU powered off) is recommended.

The full set of ISA interrupts and DMA channels are supported on the DIU ISAbus

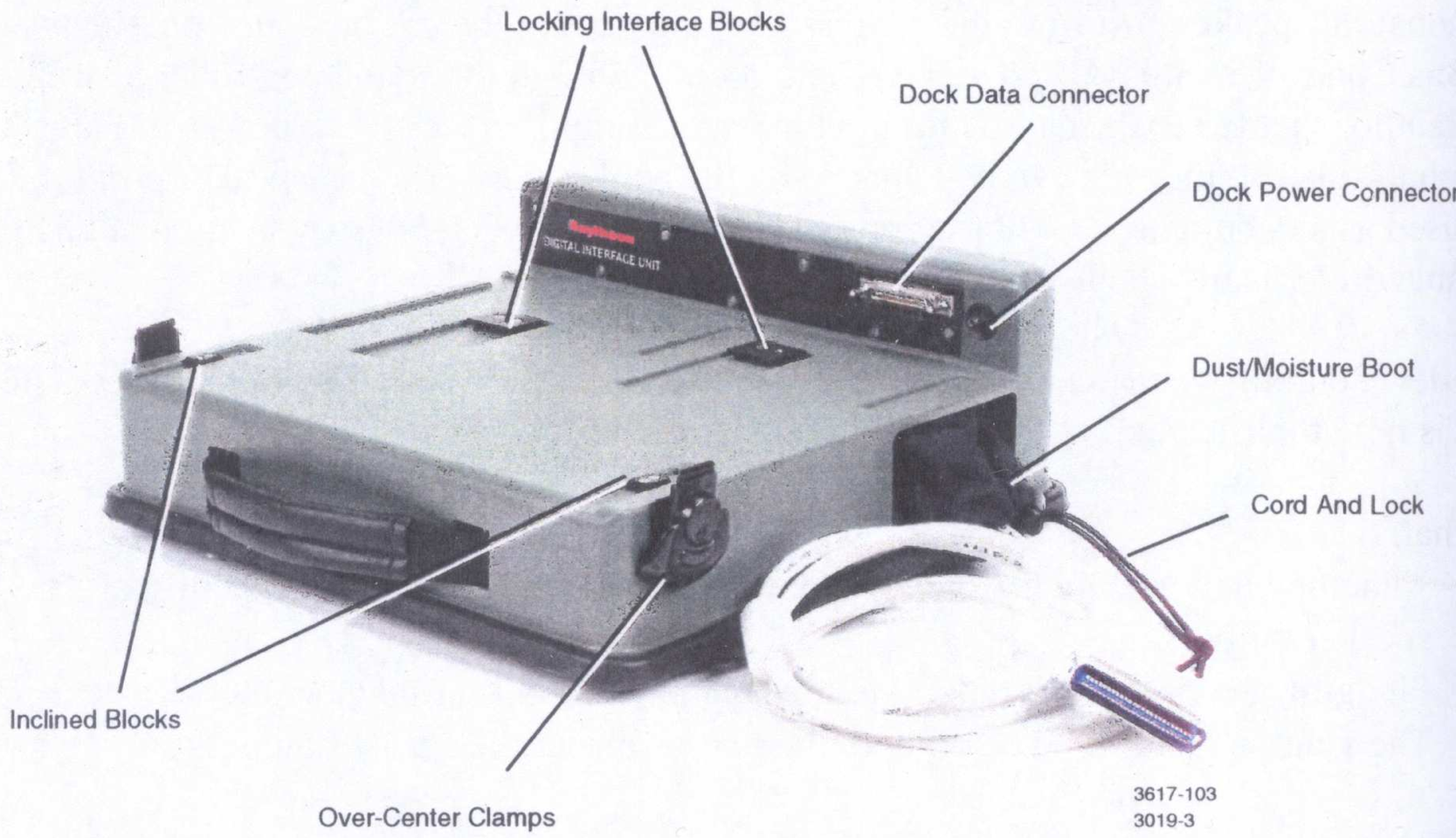


Figure 3 - DIU Front Isometric View



Figure 4 - DIU Rear Isometric View

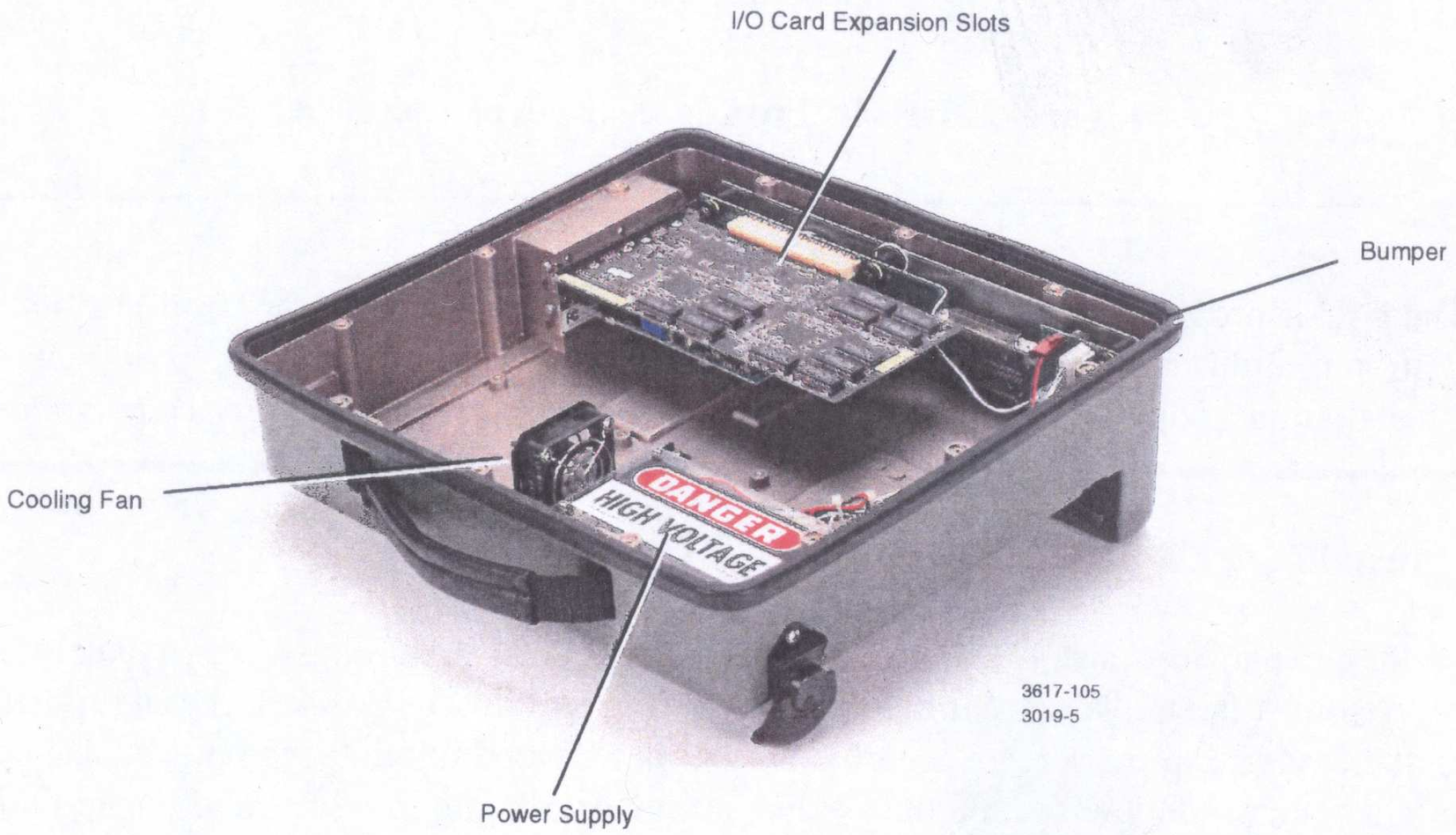
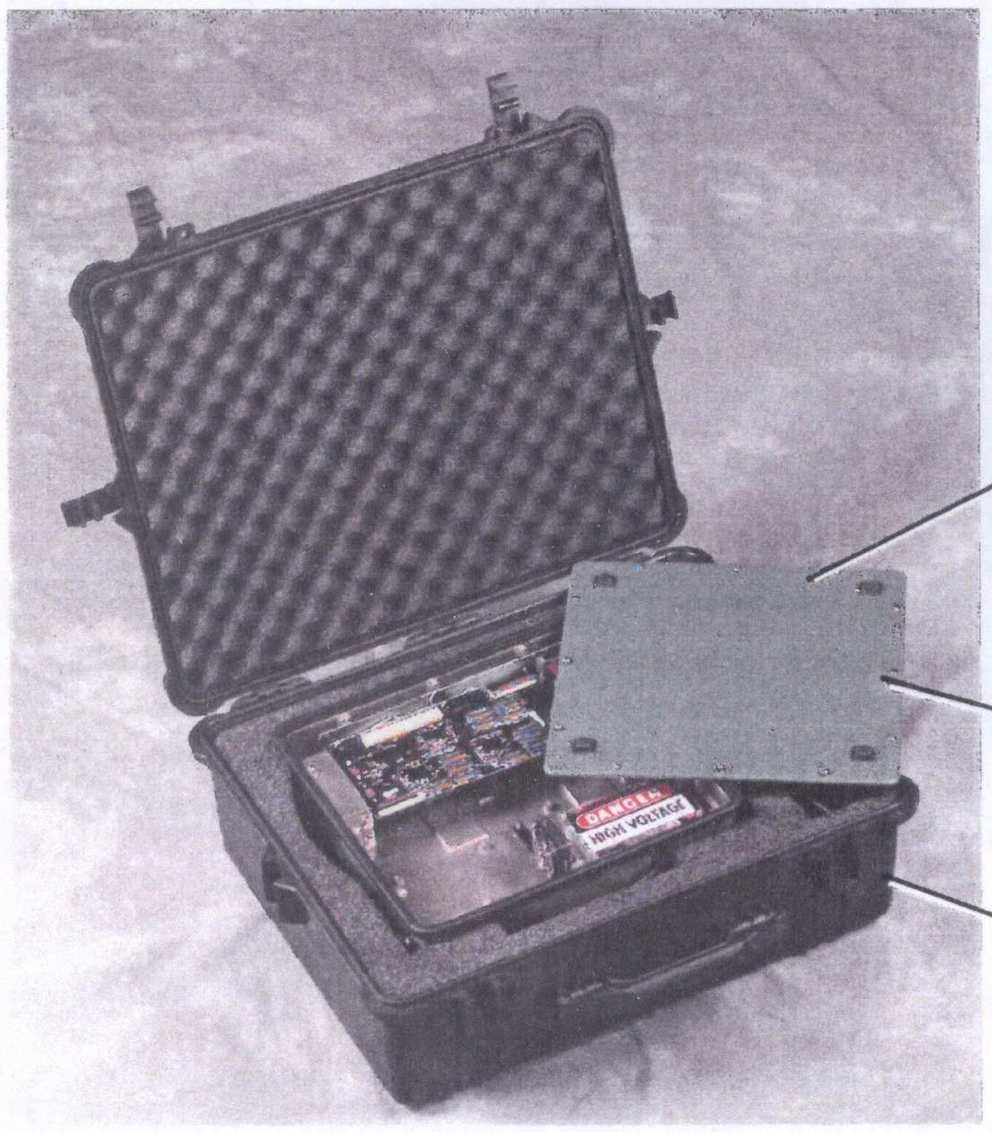


Figure 5 - DIU Internal Isometric View



3617-101
3019-6

Figure 6 - DIU in Transit case, cover removed

CAUTION

The DIU is provided with two internal PCI Card slots and two PC Card option slots for installation of industry standard PC Cards. The inside of the unit is considered Service Access only. Installation of optional internal cards is to be performed by trained service personnel only.

Installing PCI or ISA cards

To install an expansion card, the bottom cover of the DIU must be removed. An excellent holding fixture is the transit case if available, as it will hold the DIU in a horizontal position. Loosen the twelve captive screws, which hold the rear cover and bumper in place. The screws loosen in a counter-clockwise direction. When all the screws are loosened and backed out of the inserts, the cover can be removed and placed aside. This cover also holds, locates and retains the bumper.

CAUTION: ESD can damage cards if not handled properly. Make sure when handling expansion cards to avoid touching chips and circuitry.

The expansion cards are to be inserted in a vacant slot on the DIU motherboard. Hold the card (s) carefully by the edges. Install the card edge connector into the motherboard header that matches the expansion card type (either PCI or ISA). Firmly press down using the edges of the card, using equal pressure until the card is seated in the connector. Each card should be secured

using a retention screw. This screw will hold the card in place and offer support for external cables if required.

> **Note**: Any unique jumper settings should be set prior to installation of the added expansion cards.

After the cards are installed, the DIU cover should be reinstalled. This is accomplished by first verifying that the bumper is located in is mounting grove and seated all around. This can be done by firmly pressing and working the bumper all the way around the mating surface. The cover is installed by locating it on the bumper surface with the screws located above their respective inserts. The screws should be installed in a cross pattern to insure proper seating.

When the cover is installed and seated the bumper should be secure and supported evenly all around the DIU perimeter.

Attaching External Cables

If external cables are needed, the cables should be attached and accessed through the DIU boot in conjunction with the installation of the cards. The dust/moisture boot has an adjustable cord and lock that can be used after the cable is installed to provide a partial environmental. External cables should be installed with the DIU out of the transit case for ease of access.

Docking

After the desired DIU cards have been installed and the bottom cover has been reinstalled, docking can be accomplished. Power should be off and the DIU in the operational position. On each side of the DIU, position the two docking latches outward from the center of the to allow the Chameleon to be positioned. This will let the Chameleon slide into the docked position.

Align the Chameleon and DIU interface and slide the Chameleon into the docked position. There are two locking/interface feet that locate and support the Chameleon after docking. There are also two inclined blocks on each unit, which after docking, insure that the connectors are fully seated.

> **Caution**: The DIU Dock connector door needs to be removed prior to docking. Also, ensure that the dust cover and cables do not interfere with the docking surfaces.

There are two connectors, which will mate when the computer is properly docked. The digital connector locates and mates with the alignment pins/sockets. (Pins on DIU, Receiver sockets on the Chameleon). The second mating connector is the power connector. Both of these connectors have connector float for ease of docking and to provide vibration isolation.

Position the Chameleon so that sides are in line with each other. This will ensure that the locking interface feet and inclined blocks are aligned. The leading edge of the Chameleon should be approximately 1.5 ” in from of the leading edge of the DIU.

While looking at the two connectors, slide the Chameleon towards the rear of the DIU insuring that the locating pins of the data connector and the power interface connector are aligned for mating. Continue sliding the Chameleon using a slight side-to-side motion or rocking. When seated correctly, the two-locking/interface feet and inclined blocks will be aligned and seated. The final docking step is to latch the two over-center clamps on the each side of the DIU to the receivers on the Chameleon.

Over-center Clamps

To Open: Lift up the butterfly handle and rotate the handle approximately 180 degrees counterclockwise.

To Close (Chameleon in Place): Lift up the butterfly handle and swing the latch so that clamp is above the receiver on the Chameleon. This is below the two latch mounting screws. Rotate the butterfly handle in a clockwise position. When the latch is in the proper position the butterfly handle should be rotated clockwise until seated. Fold the butterfly handles down for handle storage.



Figure 7 - Chameleon / DIU docked

Power

The Chameleon and DIU in the docked position can use universal AC power through the DIU power cord. The DIU will provide power to the Chameleon for operation and for battery charging.

BIOS Setup

Setup Screens

The System BIOS setup screens and options are the standard Phoenix NuBIOS 4.06 screens with custom extensions. A legend at the bottom of each screen provides information for the user to manipulate the various setup options.

During system boot, the system runs a Power On Self Test (POST). During POST when the Rugged Mobile Computing splash screen is displayed, a message indicating that the "F2" key may be pressed to enter setup. This message is only displayed for a short time period.

Once in setup, use the up and down cursor (arrow) keys to move from field to field while the right and left arrows move from menu to menu. If the arrow keys are used to leave a menu and then return, the active field is always at the beginning of the menu. Fields with a triangle to the left are sub-menu headings; pressing Enter when the cursor rests on one of these headings opens the sub-menu. For most fields, positioning the cursor at the field and from the numeric keypad, pressing the + and - keys rotates through the available choices. Once the entry has been changed, using the up and down arrow moves to the next field.

Main Setup Menu

The Main Setup Menu is shown below:

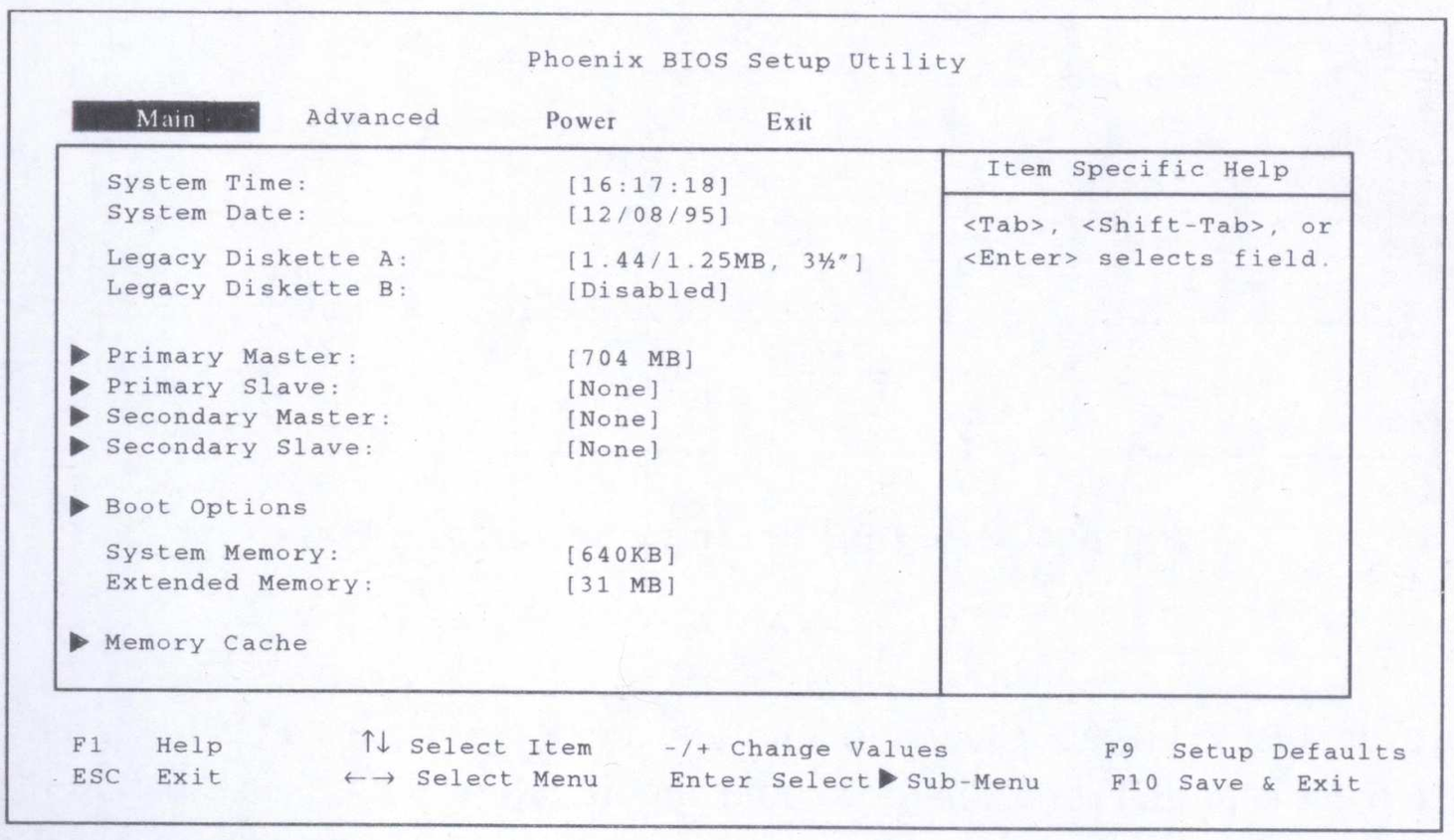


Figure 8 - (Setup) Main Menu

System Time/Date

These values are changed by moving to each field and typing in the desired entry. The TAB key moves from hours to minutes to seconds, or from months to days to years.

Legacy Diskette (A: / B)

This identifies the type of floppy disk installed as A: or B:. Possible settings are "Not Installed", and "1.44 MB, 3 ½"". The default for both A: and B: is "Not Installed".

System Memory

This field is not editable and displays the amount of conventional memory (below 1MB). No user interaction is required.

Extended Memory

This field is not editable and displays the amount of extended memory (above 1MB). No user interaction is required.

Primary/Secondary Menu

The Primary/Secondary IDE Menu is shown below.

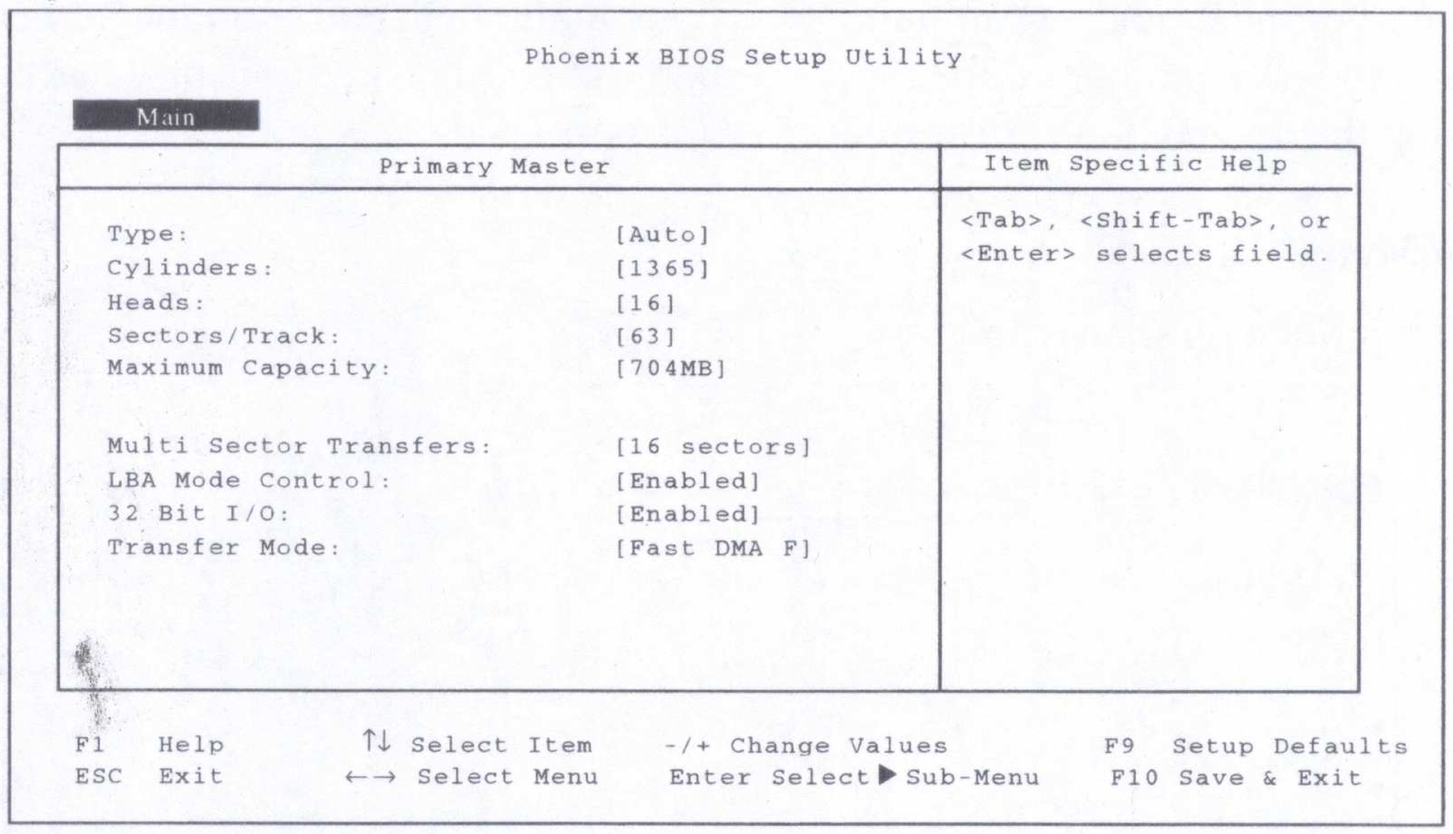


Figure 9 - (Setup) Primary/Secondary Menu

Type

"Auto" is selected if the BIOS is to autotype the device during POST. In the case for which there is an IDE disk that does not support auto-typing, then the "User" type is selected and the correct drive values for cylinders, heads, sectors/track, for the drive are entered.

Cylinders

The number of physical cylinders on the drive.

Heads

The number of physical heads on the drive.

Sectors/Track

The number of sectors that each track of the drive is divided into.

Maximum Capacity

The capacity (unformatted) of the drive.

Multi Sector Transfers

This option allows the user to configure the System BIOS to read ahead by the specified number of sectors whenever a disk access is preformed. This has the effect of reading more data at once to reduce the absolute number of discrete disk reads performed by the operating system, which may increase system performance. The possible selections are "Disabled", "2 sectors", "4 sectors", "8 sectors", or "16 sectors". Note that auto-typing may change this value if the hard disk reports that it supports block accesses. The default is "Disabled".

LBA Mode Control

When enabled, this option allows the System BIOS to reference hard disk data as logical blocks instead of using the traditional Cylinders/Heads/Sectors (CHS) method. This option can only be used if both the hard disk being configured and the operating system support logical block addressing. If disabled, then CHS mode is used. Note that auto-typing may change this value if the hard disk reports that it supports LBA. The default is "Disabled".

32 Bit I/O

This option allows the System BIOS to access the hard disk controller with 32-bit I/O access increasing system performance. This selection is not affected by auto-typing. If the onboard PCI IDE controller is used, then this option should be set to "Enabled" to maximize system performance. If an ISA bus IDE controller is installed in the system, then this option should be set to "Disabled". The default is "Enabled".

Transfer Modes

This option selects the mode that the System BIOS uses to access the hard disk. Older hard disks only support "Standard". Newer disks adhering to "Fast ATA" or "Enhanced IDE" specifications may support the fast programmed I/O or DMA modes. Note that auto-typing may change this value depending on the transfer modes that the hard disk reports it supports. The fast DMA modes take full advantage of the onboard bus mastering hard disk controller and should yield the highest performance when used in conjunction with multitasking operating systems that support it. The default is "Standard".

Boot Options Menu

The Boot Menu shown below.

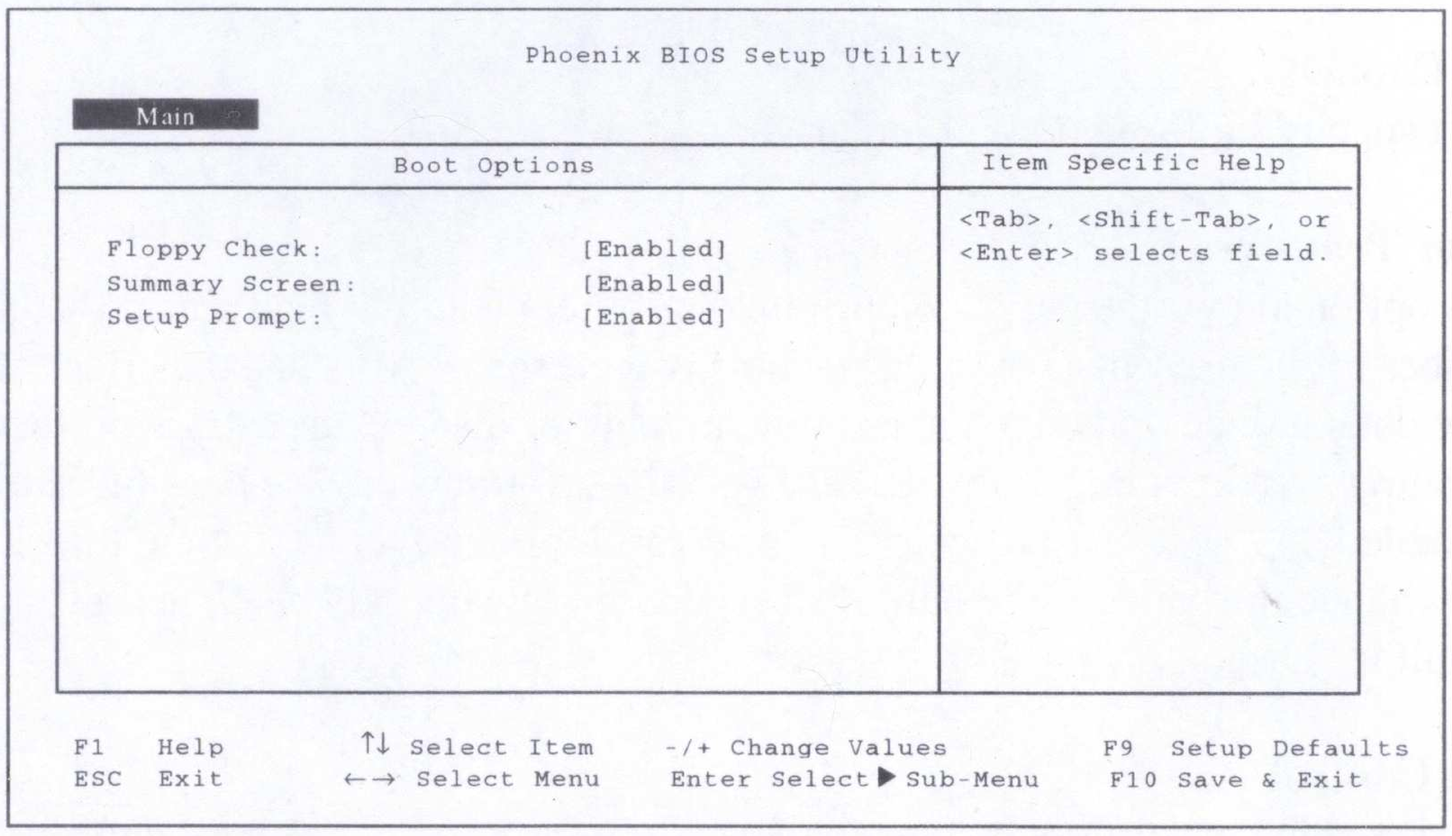


Figure 10 - (Setup) Boot Options Menu

Floppy Check

This option is used to enable or disable the floppy drive search during the boot. Setting this value to 'disabled' will speed up the boot process. It is still possible to boot from the floppy drive even though the floppy check is disabled. The default is "Enabled".

Summary Screen

This option is used to enable or disable the display of the summary screen which displays before the operation system starts to load. Setting this value do 'disabled' will speed up the boot process. The default is "Enabled".

Setup Prompt

This option is used to enable or disable the message "Press F2 to enter Setup". Even if the message is disabled, the F2 key can still be pressed at the appropriate time to enter the Setup Menu. The default is "Enabled".

Memory Cache Menu

The Memory Cache Menu is shown below.

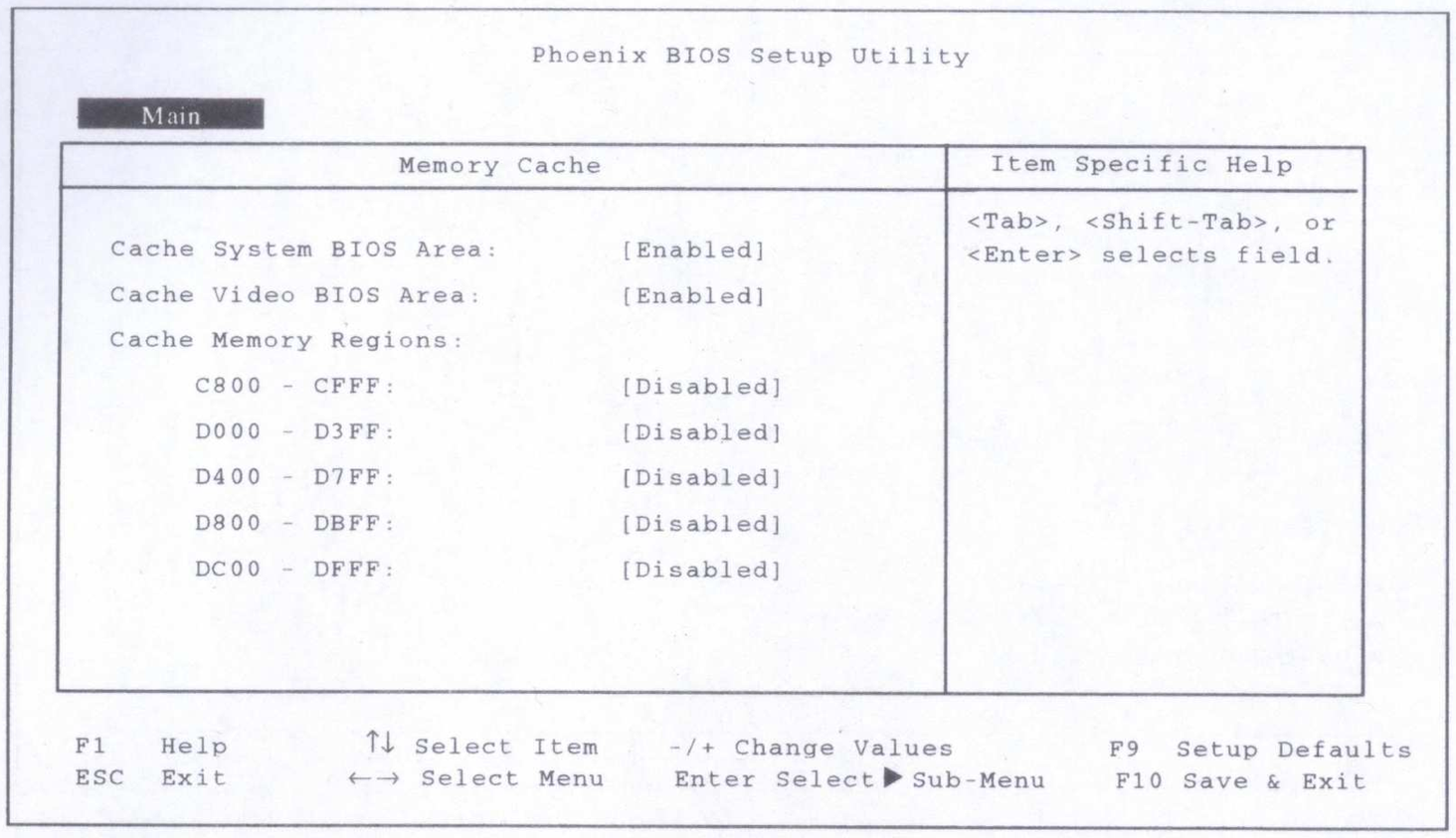


Figure 11 - (Setup) Memory Cache Menu

Cache System BIOS Area

This option enables or disables caching of the System BIOS area in the 0E0000h through 0FFFFFh DRAM area. The default is "Enabled".

Cache Video BIOS Area

This option enables or disables caching of the VGA BIOS area in the 0C0000h through 0CBFFFh region. The default is "Enabled".

Cache Memory Regions

These options enable or disable caching of the associated memory regions. When BIOS extensions are present in these regions, enabling caching for that region increases performance. The default is "Disabled".

Advanced Setup Menu

The Advanced Setup Menu contains settings for integrated peripherals, memory shadow, cache, and large disk access mode.

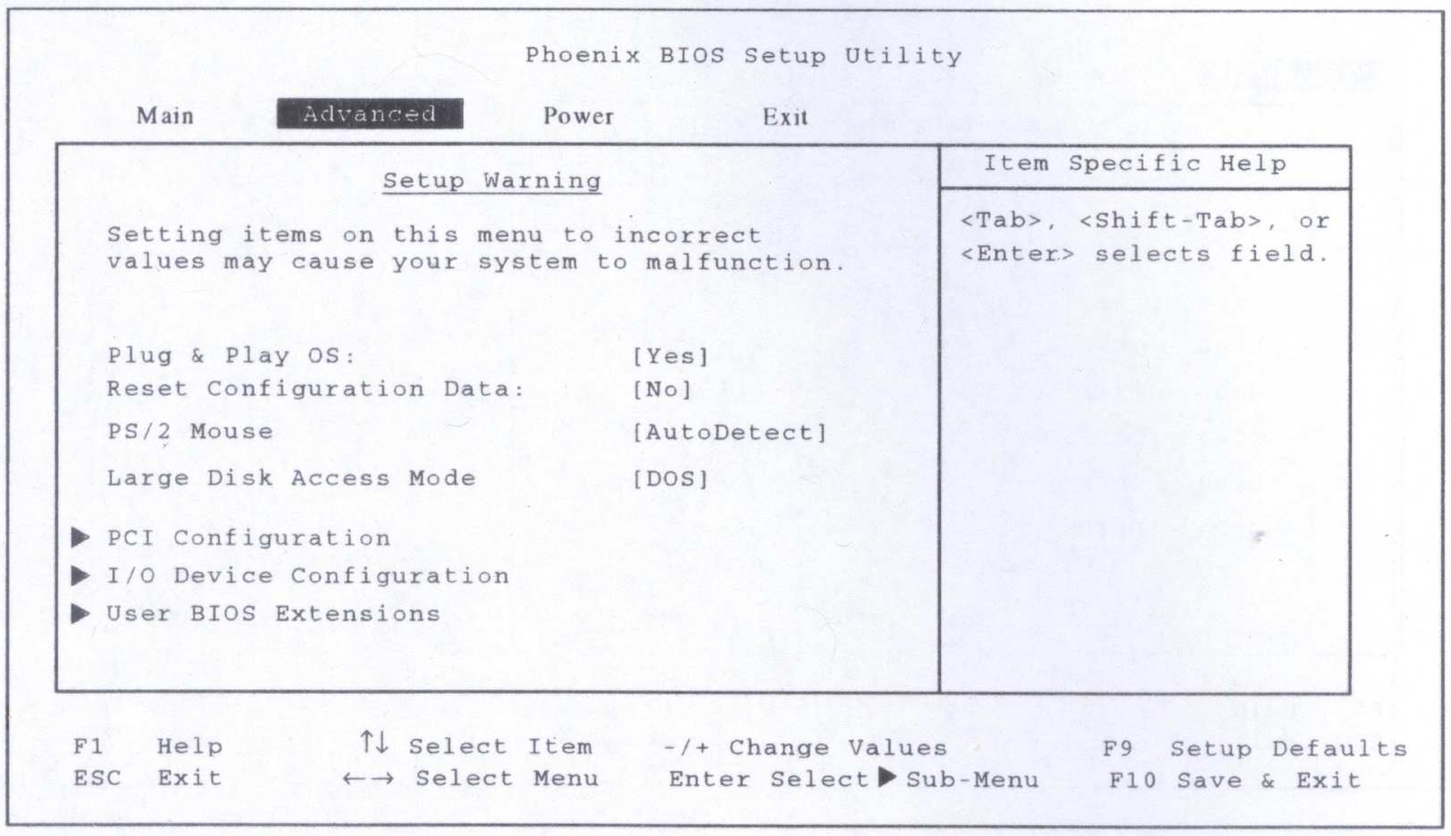


Figure 12 - (Setup) Advanced Menu

Plug & Play OS

This option informs the System BIOS whether or not the operating system being booted supports Plug and Play. If set to "Yes", the System BIOS only configures motherboard devices and those peripherals that are necessary for booting (display, hard disk, etc.). The remaining devices must be configured by the Plug and Play aware operating system. The default is "Yes".

Reset Configuration Data

If set to "Yes" the system BIOS rewrites the ESCD area in flash memory with the current system configuration data. This option is automatically reset to "No" after the ESCD is reset. The default is "No".

PS/2 Mouse

This setting either enables or disables an installed mouse. If set to "Auto Detect", the BIOS queries to find out if the mouse is installed, and if it is, the BIOS configures the mouse. With the "Auto Detect" setting, if the mouse is not found, IRQ12 is released for use by another device. The default is "Auto Detect"

Large Disk Access Mode

If a hard disk larger than 528MB is being used, this selection should be set to "DOS" if running MS-DOS, or set to "Other" if using a different operating system. When set to "DOS", this selection causes the System BIOS to perform cylinder/ head translation if the drive is configured in Setup to have more than 1024 cylinders. This allows access to hard disks up to 8GB (1024C x 255h x 63S) in size without special drivers or LBA. The default is "Other".

PCI Configuration Menu

The PCI Configuration Menu is shown below.

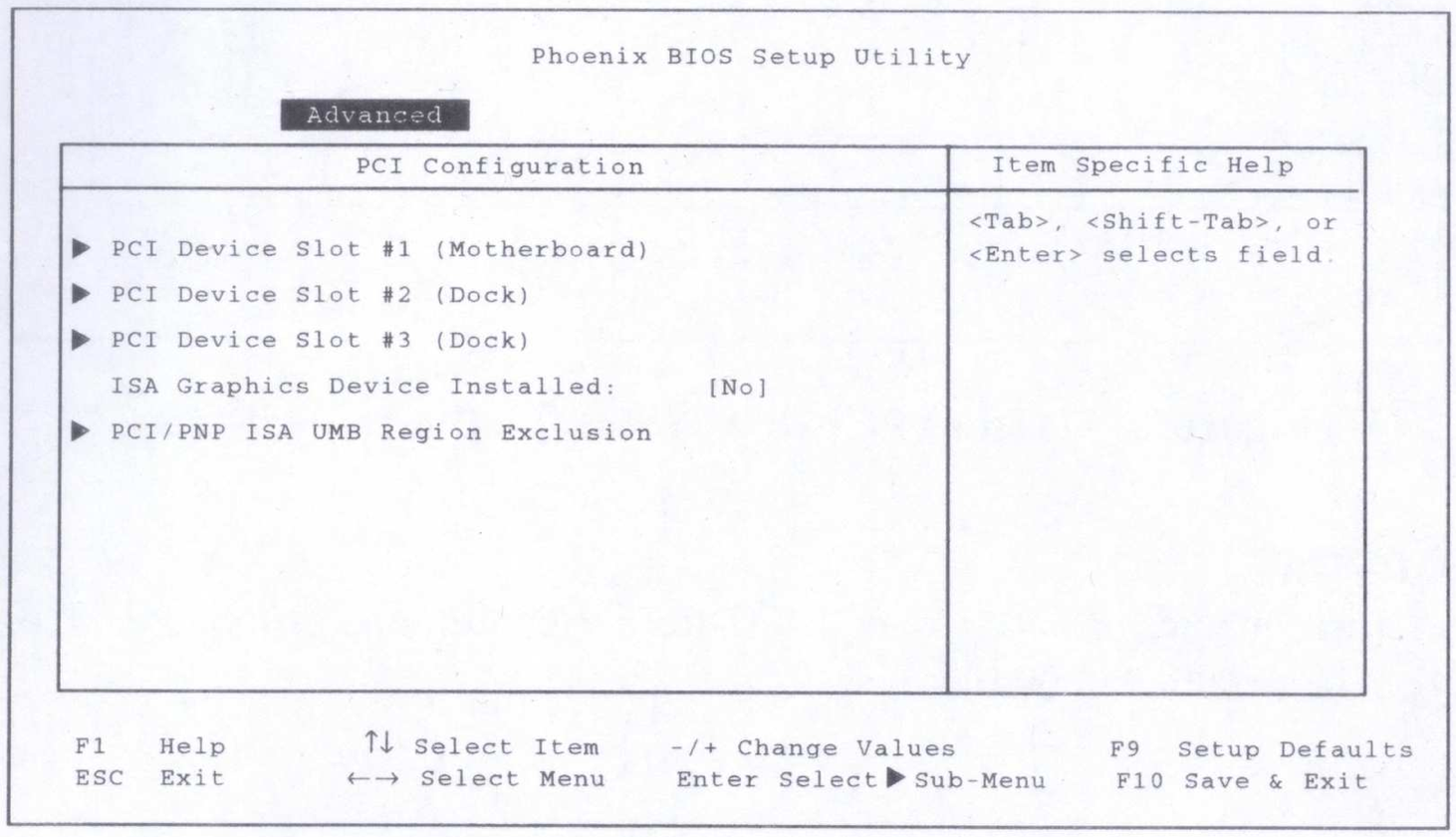


Figure 13 - (Setup) PCI Configuration Menu

ISA Graphics Device Installed

This setting informs PCI devices that there is or is not an ISA graphics device installed in the system. The default is "No".

PCI Device Slot Configuration Menu

The PCI Device Slot Configuration Menu is shown below.

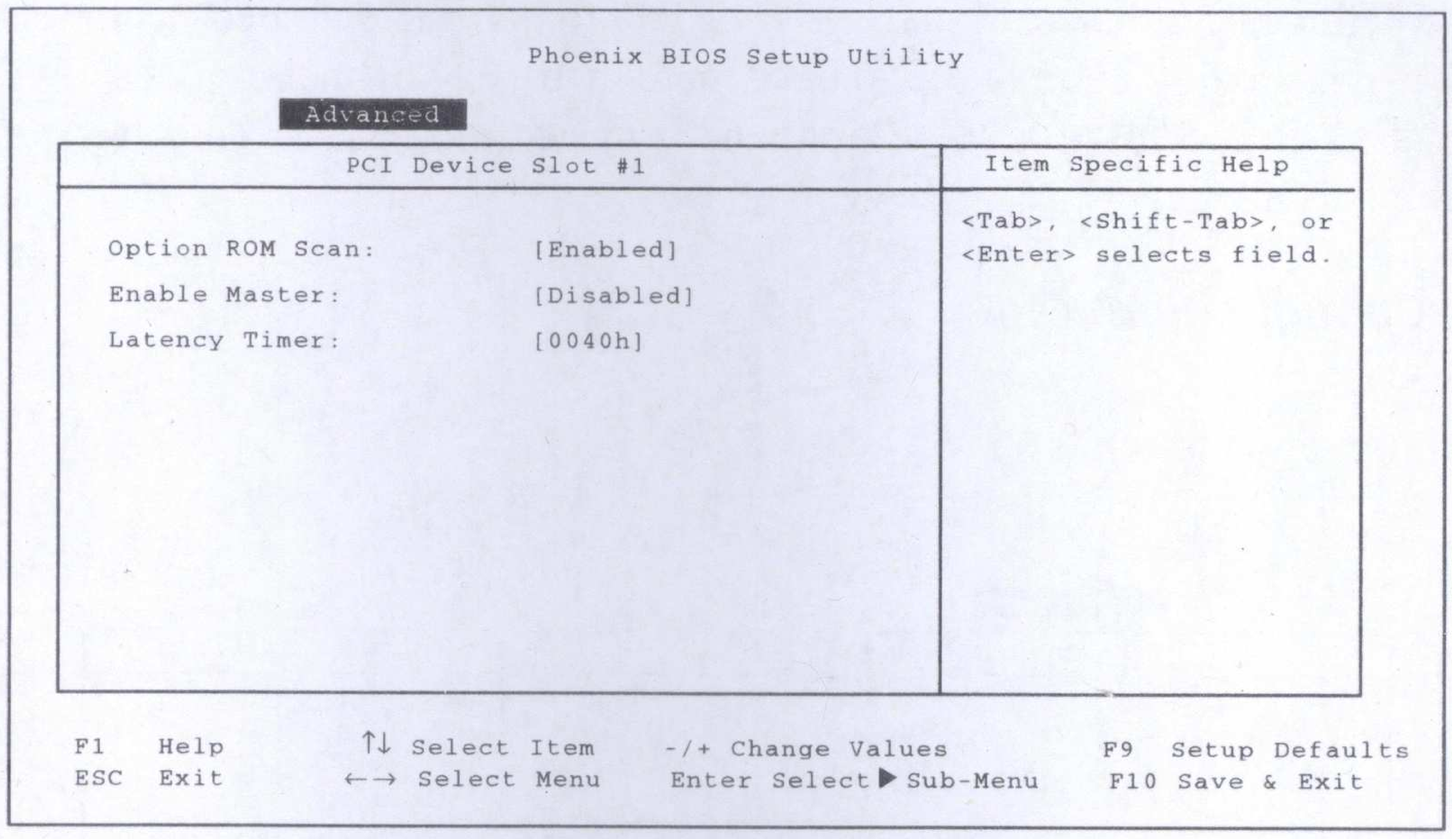


Figure 14 - (Setup) PCI Device Slot Configuration Menu

Option ROM Scan

This setting enables or disables the BIOS from executing the installed devices option ROM. The default is "Enabled".

Enable Master

This setting enables or disables the installed devices PCI bus mastering capabilities. The default is "Disabled".

Latency Timer

This setting sets the minimum guaranteed time slice for PCI bus master devices. The default is "040h".

PCI/PNP ISA UMB Region Exclusion Menu

The PCI/PNP ISA UMB Region Exclusion Menu is shown below.

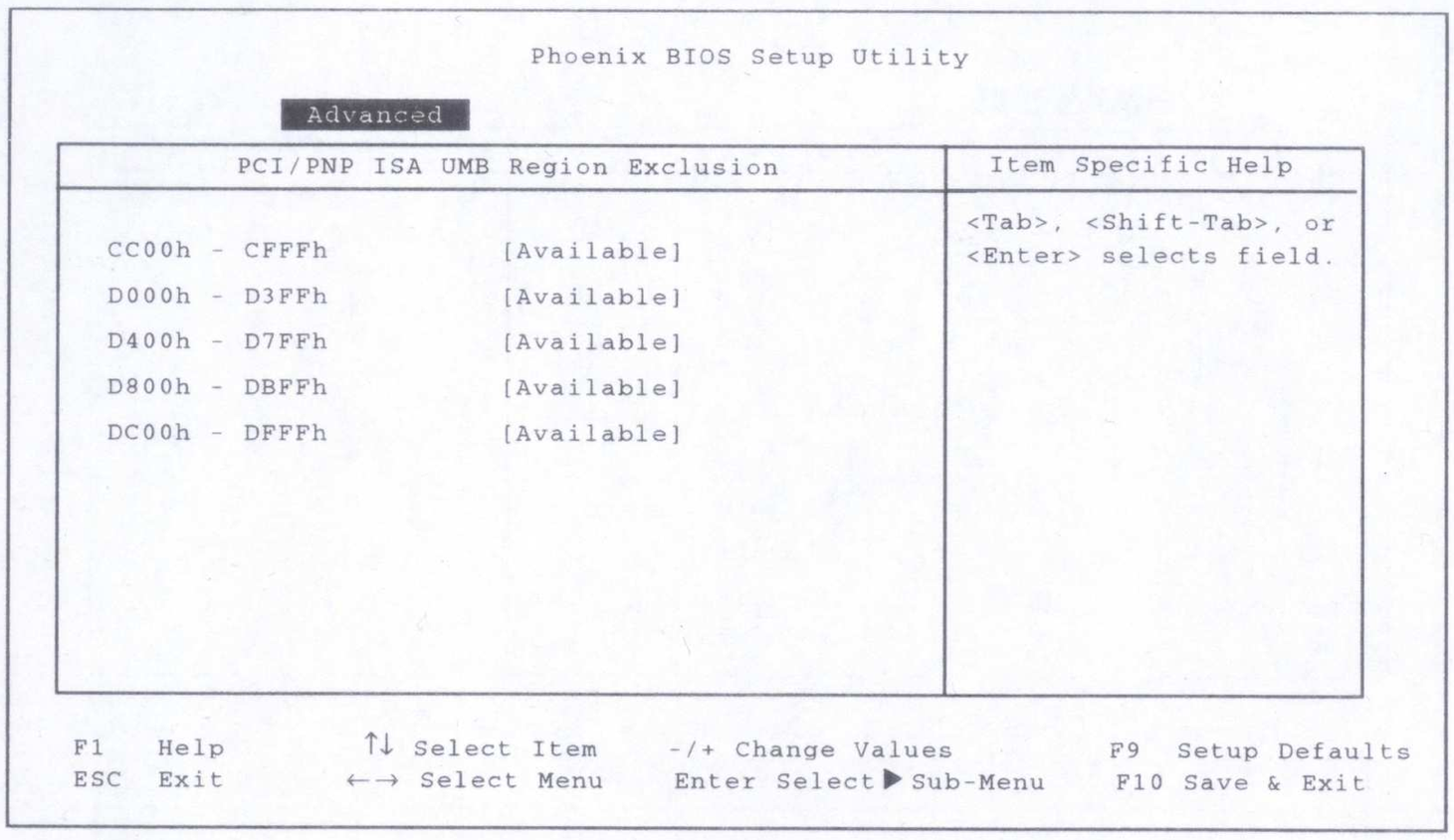


Figure 15 - (Setup) PCI/PNP ISA UMB Region Exclusion Menu

Specified Regions

This setting reserves the specified region for legacy ISA devices. If set to "Available", PCI devices may consume the indicated memory. If set to "Reserved", PCI devices may not use the specified region.

I/O Device Configuration Menu

The I/O Device Configuration Menu is shown below.

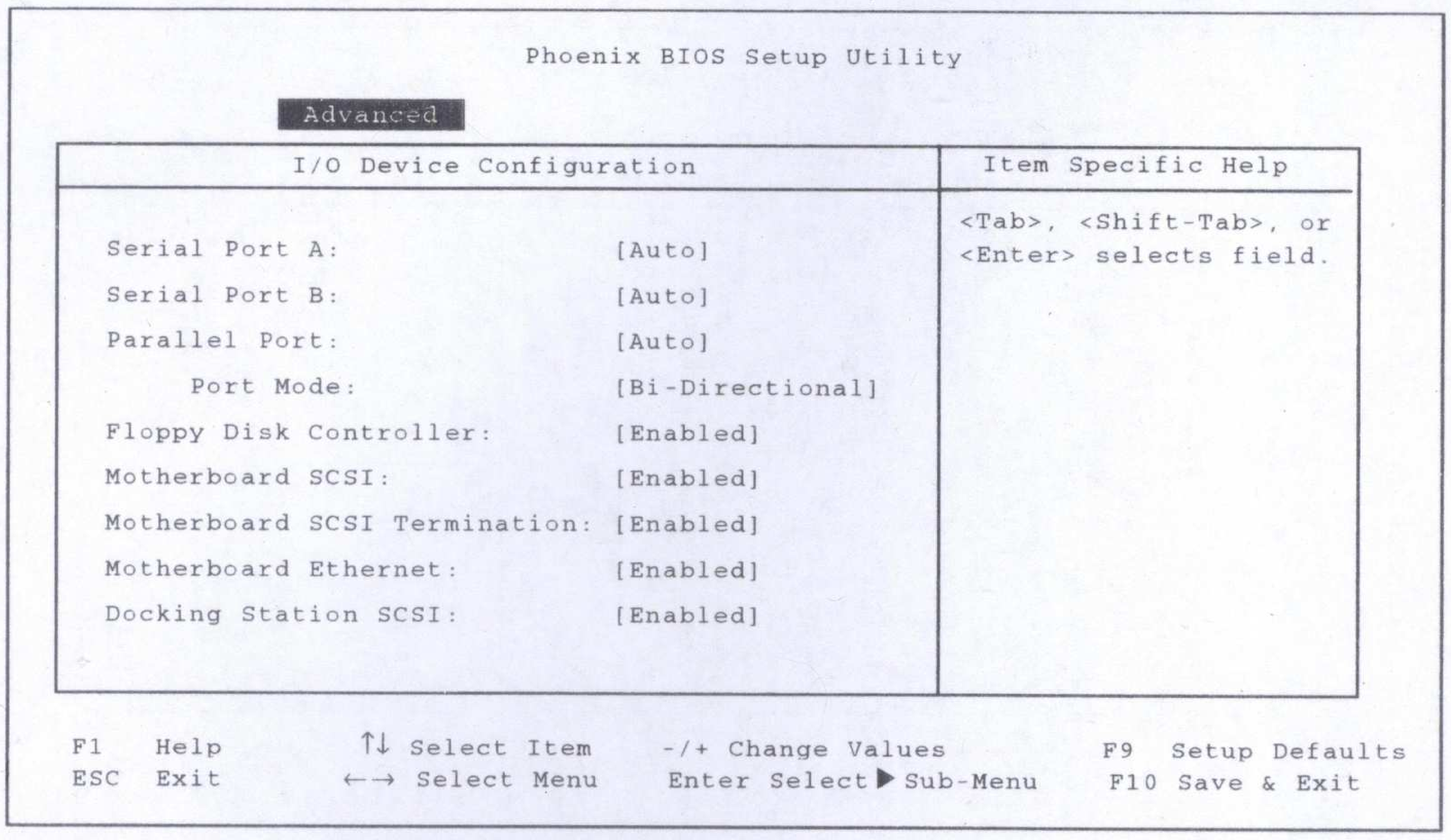


Figure 16 - (Setup) I/O Device Configuration

Serial Port A / B

This setting specifies how the serial ports are to be configured. The possible settings are "Disabled", "Enabled", or "Auto". If set to "Auto", either the BIOS or the operating system configures the ports to the best setting for the current hardware configuration. If set to "Enabled" the port may be configured by the user to one of several legacy I/O-IRQ combinations. The default is "Auto".

Parallel Port

This setting specifies how the parallel port is to be configured. The possible settings are "Disabled", "Enabled", or "Auto". If set to "Auto", either the BIOS or the operating system configures the port to the best setting for the current hardware configuration. If set to "Enabled" the port may be configured by the user to one of several legacy I/O-IRQ combinations. The default is "Auto".

Parallel Port Mode

This setting sets the mode for the parallel port using the following options: "Output Only", "Bi-Directional", "ECP", or "EPP". The default is "ECP". Note that if the port mode is set to 'ECP', the DMA channel may also be selected.

Floppy Disk Controller

This setting specifies how the floppy controller is to be configured. The possible settings are "Disabled", "Enabled", or "Auto". If set to "Auto", either the BIOS or the operating system configures the port to the best setting for the current hardware configuration. The default is "Auto".

Motherboard SCSI

This setting defines whether or not the internal (motherboard) SCSI device appears as a functioning PCI device. Disabling this device causes the SCSI controller not to appear on the PCI bus. The default is "Enabled".

Motherboard SCSI Termination

This setting defines whether or not the internal (motherboard) SCSI device is terminated. The SCSI must be terminated if no additional SCSI devices will be chained to this controller. The default is 'Enabled'.

Motherboard Ethernet

This setting defines whether or not the internal (motherboard) Ethernet device appears as a functioning PCI device. Disabling this device causes the Ethernet controller not to appear on the PCI bus. The default is "Enabled".

Docking Station SCSI

This setting defines whether or not the external (docking station) SCSI device appears as a functioning PCI device. Disabling this device causes the SCSI controller not to appear on the PCI bus. The default is "Enabled".

User BIOS Extension Menu

The User BIOS Extension Menu is shown below.

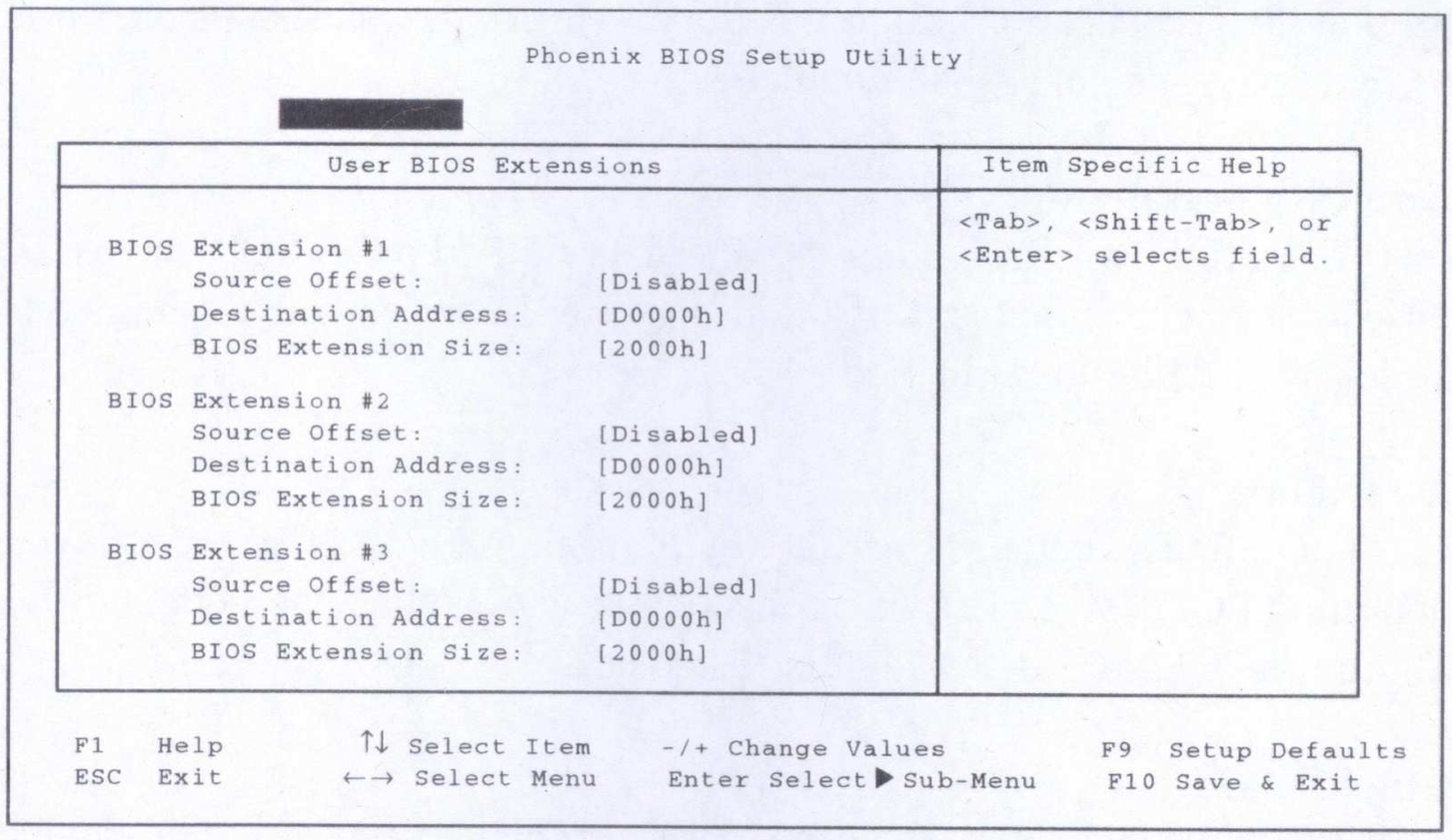


Figure 17 - (Setup) User BIOS Extension Menu

Source Offset

This option selects the source address of the BIOS extension located in the FBD. The address is an offset from the base of the FBD. The offset range is between 0000h and 18000h in 8KB increments. The default is "Disabled".

Destination Address

This option selects the target address of the BIOS extension which can range from CC000h through DFFFh in 8KB increments. The default is "D0000h".

BIOS Extension Size

This option selects the number of bytes to copy from the FBD into shadow memory. BIOS extension sizes can be selected in 8KB increments from 2000h to 10000h. The default is "2000h".

Power Management Menu (APM 1.2)

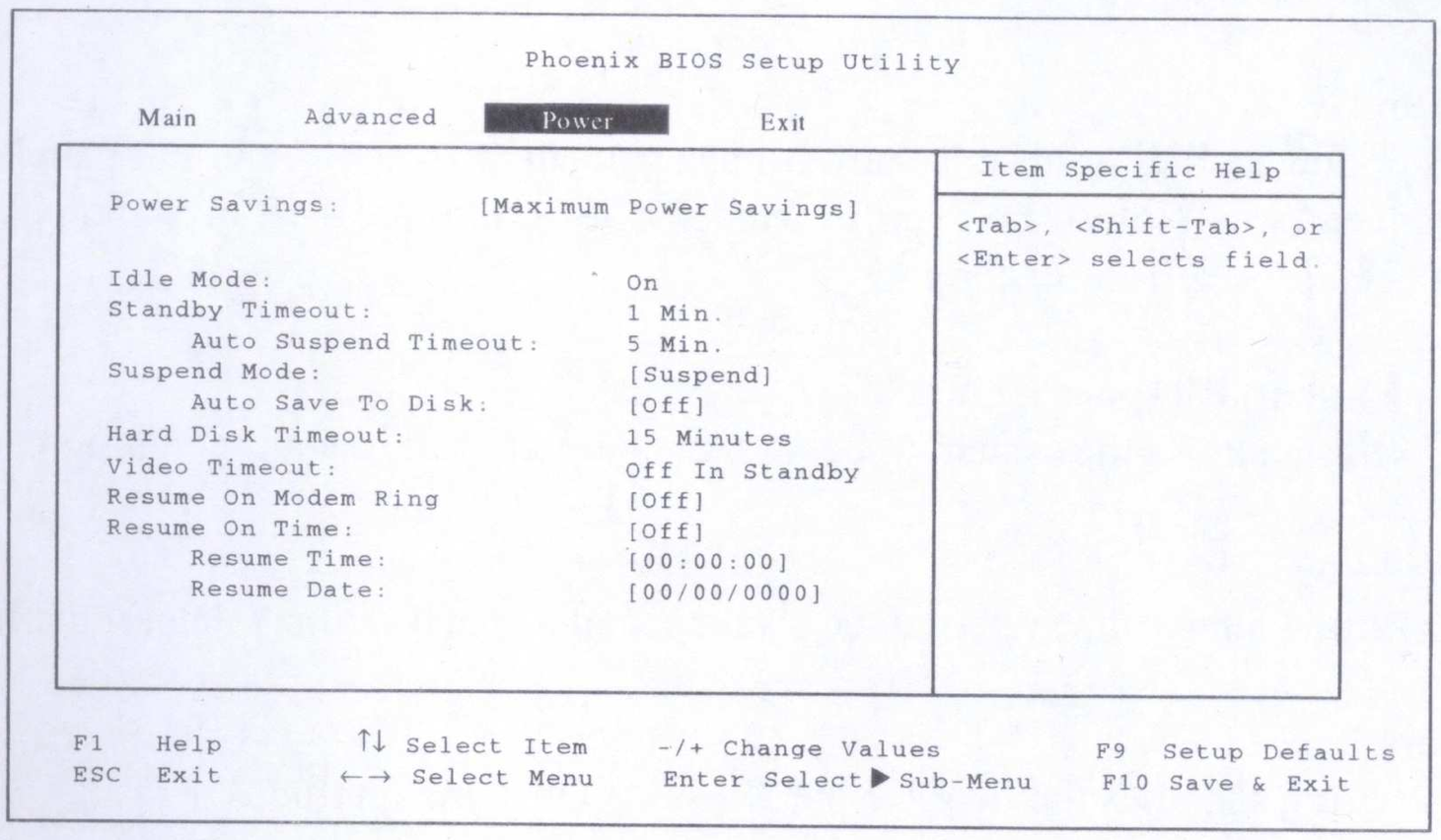


Figure 18 - (Setup) Power Management Menu

Power Savings

This option enables and selects the kind of power management, or it disables power management. The options are "Customize", "Maximum Power Savings", "Medium Power Savings", "Minimum Power Savings", and "Disabled". The default is "Customize".

Idle Mode

This setting turns on or off the Idle Mode (clock throttling) power saving switch. Clock throttling slows down the processor (and thus saves power) during brief periods of reduced activity.

Standby Timeout

This option enables and sets the inactivity duration required to elapse before the system is placed into Standby Mode, or it disables the Standby Timeout. The options are: "Disabled", "2 min.", "15 min.", "30 min.", "1 hour", "2 hours", "3 hours", and "4 hours". The default is "15 min."

Auto Suspend Timeout

This setting specifies the amount of time that the system must be in standby mode before it may enter suspend mode.

Suspend Mode

This setting selects the type of suspend mode.

Hard Disk Timeout

This option enables and sets the inactivity duration of fixed disk accesses required to elapse before the system shuts off the disk drive or it disables the Fixed Disk Timeout.

The options are "Disabled", "1min", "2 min", "3 min", "4 min", "5 min", "10 min", and "16 min." The default is "15 min."

Video Timeout

This option enables or disables power management of the CRT and flat panel during system entry/exit into/from Standby Mode. The options are "Off in Standby", and "On". The default is "Off in Standby."

Resume On Modem Ring

This setting allows the system to be awakened upon receiving an incoming call.

Resume On Time

This setting allows the system to be awakened at a specific time / date in the future.

Resume Time

This setting specifies the time for the "Resume On Time" setting.

Resume Date

This setting specifies the date for the "Resume On Time" setting.

Exit Menu

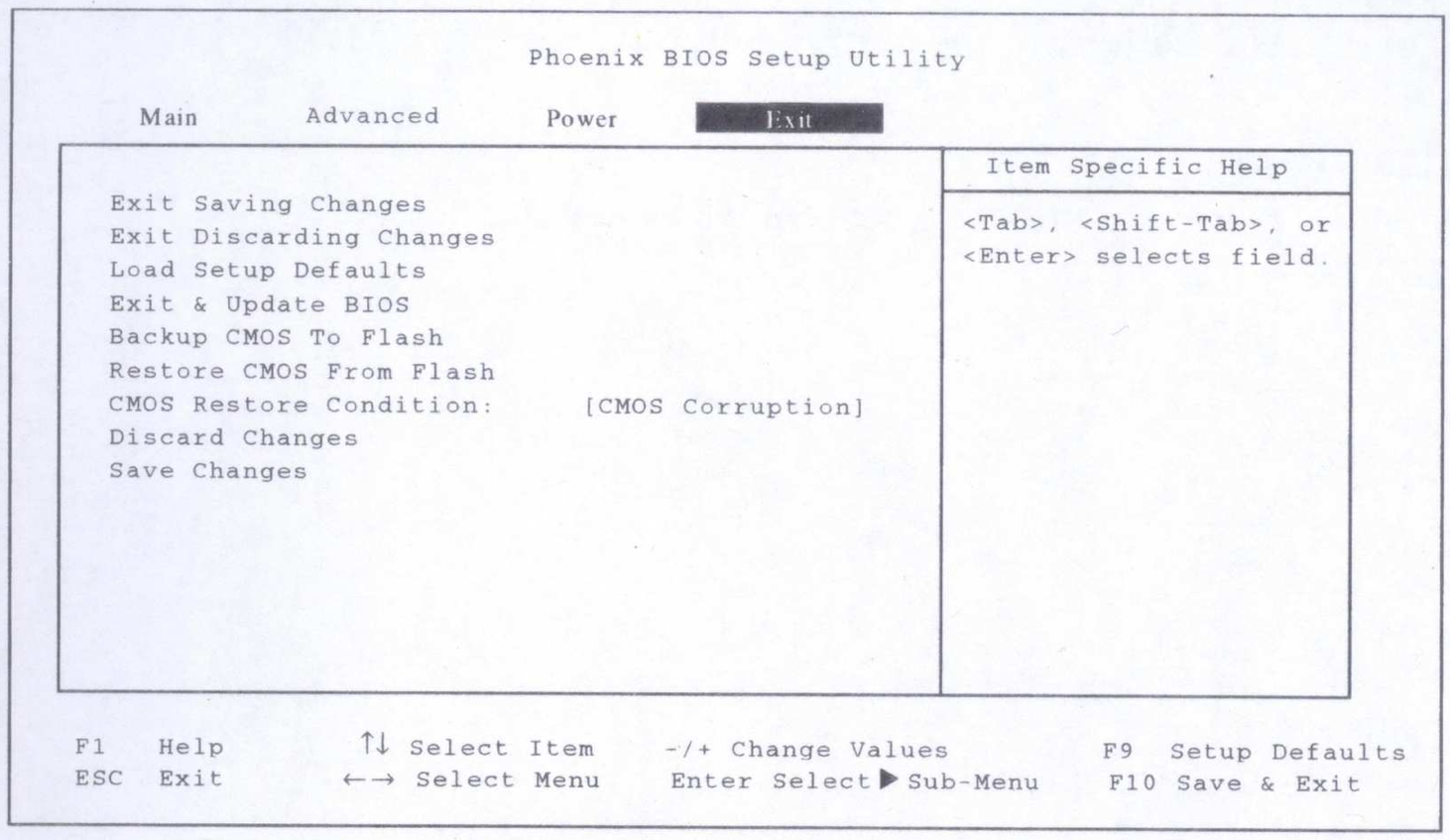


Figure 19 - (Setup) Exit Menu

Exit Saving Changes

This option is used to save into CMOS the values that have been entered and to reboot the system.

Exit Discarding Changes

This option is used to discard the changes just made and revert to the state when Setup was entered. The system reboots with the old values.

Load Setup Defaults

This option is used to reset the Setup values to the original default values that were set at the factory.

Backup CMOS To Flash

This option is used to save the current Setup values to flash memory.

Restore CMOS From Flash

This option is used to restore previously saved Setup values from flash memory into CMOS.

CMOS Restore Condition

This option sets under what condition the System BIOS reloads CMOS from flash memory. The options are “Always”, “Never”, and “Corrupt CMOS”. The default value is “Never”.

Discard Changes

This option is used to disregard the recent changes that were made to setup values and to restore them to the values that were in effect when the user entered Setup.

Save Changes

This option is used to save the current Setup values into CMOS.

Exit & Update BIOS

This option is used to initiate a System BIOS update.

Software Support

Phoenix NuBIOS 4.06

The system BIOS is based on the Phoenix NuBIOS version 4.06 implemented as a Flash BIOS using the Intel 28F400B5-T Boot Block Flash Device (hereafter referred to as the Flash Boot Device or FBD). The system boot block code resides in the upper 16KB block, parameter block #2 is reserved for the Plug and play BIOS's extended system configuration data (ESCD) area, and parameter block #1 is reserved for CMOS save and restore (CSR) data. The system BIOS code and data as well as the VGA BIOS, and a manufacturing BIOS extension reside in main blocks #4 and #3. Main block #1 is reserved for storage of User BIOS Extensions. Main block #2 is unused.

The boot block is protected against accidental writes by a jumper which, if installed, allows writes to the boot block. This "switch" (BB_ENB) is provided on the CPU motherboard to avoid having to unsolder the FBD. In addition to the hardware protection of the boot block, the entire FBD is write protected via a write enable bit in one of the chipset registers. Since this register resides in the PCI configuration address space of the PIIX4, unintentional writes to it are unlikely.

The System BIOS provides Plug and Play configuration and runtime services for operating systems that can utilize them. This functionality is provided in a separate code module (the PTLPNP 4.2 code base) obtained from Phoenix Technologies and is compliant with the Plug and Play BIOS specification 1.0a.

The System BIOS supports Phoenix desktop power management (APM 1.2 compliant) which is a subset of the Advanced Power Management (APM) features found on portable PCs. In particular, save and resume from disk are not supported.

The System BIOS also supports a subset of ACPI 1.0.

For various reasons, this system will not meet PC97 or PC98 specifications and no attempt has been made to acquire formal Microsoft labeling.

The Flash Boot Device is organized according to the following diagram:

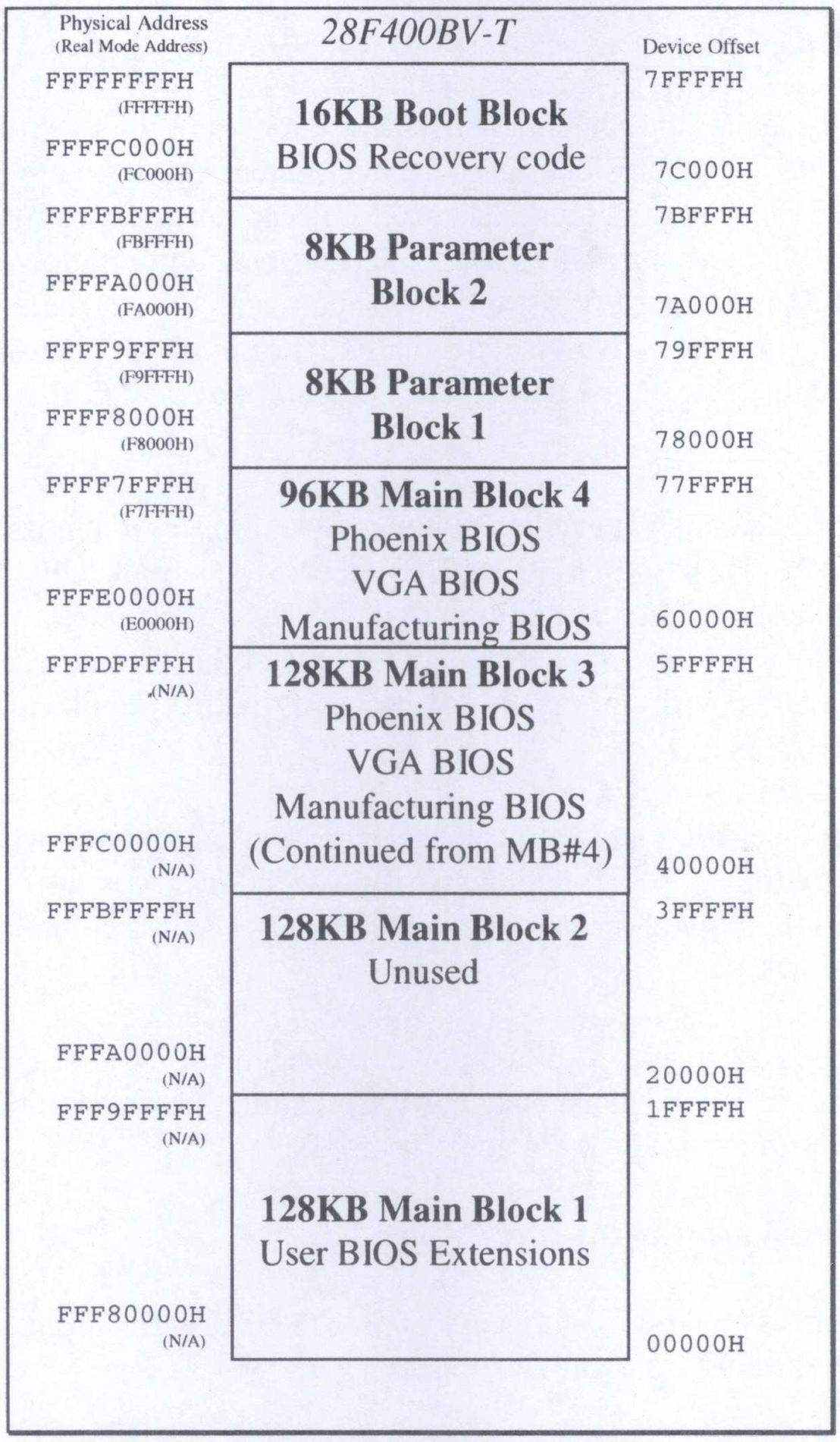


Figure 20 - Flash Boot Device Memory Map

Flash Boot Device Reflashing

The System BIOS is updated by using a special boot diskette that contains code to perform the update as well as the System BIOS image itself. The floppy update mechanism is standard to the Phoenix NuBIOS and requires that a standard PC floppy diskette drive be functional in the system. References in this section to "MS-DOS" refer to MS-DOS® 6.22 or the Windows® 95 command line interface available during the boot process before the Graphical User Interface (GUI) is started. There is no native reflashing support for other protected mode operating systems such as Windows NT®, OS/2®, QNX®, etc. Flash boot device reflashing must be accomplished by Raytheon service personnel.

CMOS Save and Restore (CSR)

The user is allowed to save and restore a setup configuration (CMOS) into flash memory. This feature is useful in the event of battery failure or corrupt CMOS RAM. Also, this feature allows systems without batteries to boot properly while still allowing the user to configure the system via Setup. Restoration of CMOS from flash memory can be either automatic or manual through the setup exit menu.

The CMOS RAM configuration backup is stored in FBD parameter block #1 (8KB). This entire block is reserved for this purpose and cannot be shared.

The user selects to backup or restore the current CMOS RAM configuration from the Exit setup menu. CSR does not automatically backup CMOS RAM but relies on the user to do so via Setup.

The available selections from the Exit setup menu that would force a CMOS restoration are: *Always* restore, *Never* restore, and restore on *Corrupt CMOS*. The default setting is *Never*.

BIOS Extensions

BIOS extensions located in the region 0CC000h through 0DFFFFh on the PCIbus or ISAbus are not automatically shadowed by the System BIOS, but manually through Setup menu items. Shadowing a region automatically write-protects it. If a BIOS extension is not shadowed, accesses to its address space are routed through the ISAbus directly to the ROM. Note that by definition, PCI BIOS extensions must be shadowed and exist in upper memory.

BIOS extensions cannot be located in the 0E0000h through 0EFFFFh region since this interferes with the Plug and Play and PCI BIOS code already shadowed there. BIOS extensions cannot be located in the 0C0000h through CBFFFh since the VGA BIOS extension consumes this region.

User BIOS Extensions

The FBD reserves a 128KB block (main block #1) to be used for BIOS extension storage. In order to use this area for BIOS extensions, it is first necessary to program the image into the FBD (using REFLASH.EXE) and then, at run time, copy the BIOS extension from the FBD into DRAM, and have the System BIOS scan that region for BIOS extensions. Multiple BIOS extensions can be programmed into this block of the FBD. Setup items in the Advanced menu allows the user to select which BIOS extensions are shadowed during POST.

Machine ID

The System BIOS contains a machine identification structure which contains the system identification number 78 (4Eh) and a major and minor revision number which are displayed in the cold start banner.

Boot Block ID

The boot block contains a boot block identification footprint structure which contains a major and minor revision number which are displayed in the cold start banner.

ACPI Support

Definition of ACPI States

The following section defines the complete compliment of ACPI states (global, processor, device, and sleeping) implemented for this system. The ACPI support included in the BIOS is only accessible by an ACPI aware operating system. Non-ACPI aware operating systems must rely on the BIOS support of the APM 1.2 specification.

Global States

G0 State: This is defined as the "working" state. The machine is fully functional and executing user code. System devices (Ethernet / SIO / VGA / …) may be power managed depending on implementation. CPU clock throttling (see processor states below) is used to reduce power consumed by this device during brief periods of inactivity.

G1 State: This is defined as the "sleeping" state. User applications are not being executed, and the machine appears to be off. Large elements of the system context are saved by hardware. Return to the G0 state can be accomplished without rebooting the system.

G2 State: This is defined as the "soft-off" state. No user mode code is being executed. A return to the G0 state is accomplished via a system reboot. This is the state that the computer is in after accomplishing a normal Windows shutdown.

G3 State: This is defined as the "mechanical off" state. No electrical current is running through the circuitry. No system context is saved, and a return is only accomplished via a full reboot of the system. The mechanical off state is when the battery pack is removed and not line power is connected.

Processor States

C0 State: In this state the processor operates at full power and executes instructions normally.

C1 State: CPU instructions are not executed in this state. The latency to return to the C0 state is small enough that operating system software does not consider the C1→ C0 transition.

C2 State: CPU instructions are not executed in this state. The latency to return to the C0 state is longer than the previous (C1) state, and ACPI tables inform the operating system of this increased latency.

C3 State: CPU instructions are not executed in this state. The latency to return to the C0 state is longer than the previous (C2) state, and ACPI tables inform the operating system of this increased latency. The Processor's cache must be invalidated when returning to C0 from this state.

Device States

D0 State: This state is defined as "full on". In this state the device provides full functionality, maintains context in hardware, and consumes maximum power.

D1 State: Many device classes do not support this state. In this state the device consumes less power than in the D0 state. The device context maintained by the device in this state is expected to be less than in the D0 state but greater than the D2 state.

D2 State: Many device classes do not support this state. In this state the device consumes less power than in the D1 state. The device context maintained by the device in this state is expected to be less than in the D1 state.

D3 State: This state is defined as "full off". The device is not expected to maintain any context.

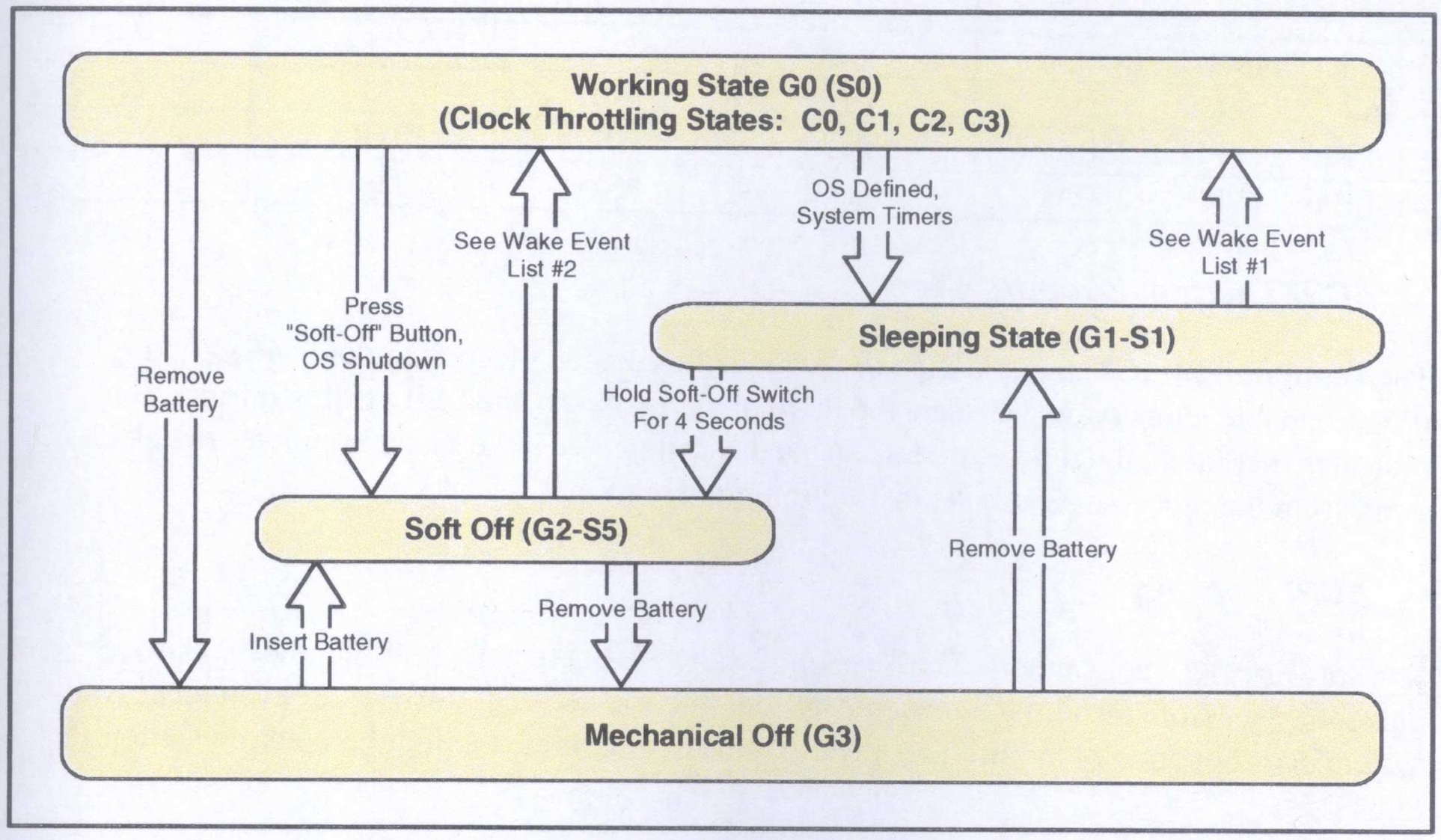
System Sleep States

S1 State: The latency for return to the G0 state from this state is defined to be a minimum. All system context is maintained in hardware.

S5 State: This state is defined as "soft off". Upon wake from this state, the system requires a complete reboot.

Scope of ACPI Support

The usage model for this product has been specified as either "all on" or "all off". Under this model, use of ACPI power management is limited, however some of the ACPI power management functionality is implemented to reduce power consumption without affecting expected performance. The following figure depicts the supported states. Note that the numbered lines indicate state transition vectors and are explained below.



3019-9

Figure 21 - ACPI State Diagram

Wake Event List #1:

The following events cause the system to be awakened from the Sleeping (G1-S1) state.

- RTC Alarm
- SMBus access
- Power Management Resume Enable (PME#) Events
- Soft-Off Power Button (less than 4 seconds)
- Interrupt Events
- USB

Wake Event List #2:

The following events cause the system to be awoken from the Soft-Off (G2-S5) state.

- RTC Alarm
- Soft-Off Power Button (less than 4 seconds)

ACPI Supported Devices

The following table enumerates the ACPI device level support for each of the listed devices. The interface to each of these devices is provided to the operating system via ACPI Source Language (ASL) incorporated into the BIOS

Table 3. Device Level ACPI Support

Device	Supports ACPI D0	Supports ACPI D1	Supports ACPI D2	Supports ACPI D3
Ethernet (Intel 82558)	Yes	Same As D0	Yes	Yes
VGA (C&T 69000)	Yes	No	No	Yes
Card Bus 1 (TI PCI1250A)	Yes	TBD	TBD	Yes
Card Bus 2 (TI PCI1250A)	Yes	TBD	TBD	Yes

ACPI Thermal Support

The Pentium II MMC-2 module includes a single thermister attached to the SMBus. At programmable temperature settings, the thermal alarm asserts the SMI. If this information indicates that internal temperature has reached a critical level, the system removes the clock input from the processor and halts instruction processing.

ACPI Docking

The software does not support "Hot Docking", however there is no physical mechanism to prevent a user from installing a powered system into the dock. If this type of event occurs, the system does not attempt to initialize any of the devices that are behind the docking station PCI-PCI bridge.

The software does support "Cold Docking". Cold Docking is defined as an insertion of the laptop into the docking station while the laptop is in the soft-off state. On the next boot cycle, the system enumerates and configure any devices that are behind the PCI-PCI bridge on the docking station (including ISA devices).

Software Miscellaneous

Phoenix NuBIOS Checkpoints

The following table provides the check point codes that the system BIOS emits to port 80 during POST. Note that the checkpoints are listed in ascending order and are not necessarily in order of execution.

Beep Codes:

If an error occurs at any of the below listed check points, the system attempts to emit a beep code to indicate where the error occurred. Beep codes may be derived from the "Post Code" column in the following manner: The "Post Code" byte is first broken down into four - two bit tokens. These tokens are then made one-based. These four - two bit tokens are then emitted via the speaker MSB first.

Example: Post Code = 01Ch (Reset Programmable Interrupt Controller)

01Ch = 00011100b → 00 01 11 00

Now, adjust to a 1 based system to yield a beep code of 1-2-4-1

Table 4. NuBIOS CheckPoint Table

Post Code	Checkpoint Description
002H	Verify Real Mode
003H	Disable Non-Maskable Interrupt
004H	Get CPU Type
006H	Initialize System Hardware
008H	Initialize Chipset Registers With Initial POST Values
009H	Set Flag Indicating System Is In Post
00AH	Initialize CPU Registers
00BH	Turn CPU Cache On
00CH	Initialize Cache
00EH	Initialize I/O Device(s)
00FH	Initialize Fixed Disk
010H	Initialize Power Management
011H	Load Alternate Registers With Initial Post Values
012H	cpuRestoreCR0J
013H	Issue PCI Bus Master Reset
014H	Initialize Keyboard Controller
016H	Checksum The BIOS
017H	Autosize Cache
018H	Timer Initialization
01AH	DMA Initialization
01CH	Reset Programmable Interrupt Controller

Post Code	Checkpoint Description
020H	Test DRAM Refresh
022H	Test Keyboard
024H	Set ES Segment Register To 4GB
028H	Autosize DRAM
029H	Initialize Phoenix Memory Manager
02AH	Clear 512KB Base RAM
02CH	Test 512KB Base Address Lines
02EH	Test Low Byte Of 512KB Base Memory
02FH	Enable CPU Cache
032H	Establish CPU Bus Clock Frequency (CPU Speed)
033H	Initialize Phoenix Dispatch Manager
036H	Check Shutdown Code
038H	Shadow System BIOS
03AH	Autosize System Cache
03CH	Configure Advanced Chipset Registers
03DH	Load Alternate Chipset Registers With CMOS Values
042H	Initialize Interrupt Vectors
045H	Initialize PNP Devices
046H	Check ROM Copyright Notice
048H	Check Video Configuration Against CMOS
049H	Initialize PCI Bus And PCI Devices
04AH	Initialize All Video Adapters
04BH	Start "QuietBoot"
04CH	Shadow Video BIOS ROM
04EH	Display Copyright
050H	Display CPU Speed/Type
051H	Initialize EISA Board(s)
052H	Test Keyboard
054H	Initialize Keyclick Features
058H	Test For Unexpected Interrupts
059H	Initialize Phoenix Display Manager
05AH	Display "Press F2 To Enter Setup" Message
05BH	Turn CPU Cache Off
05CH	Test RAM Between 512KB And 640KB
060H	Test Extended Memory
062H	Test Extended Memory Address Lines
064H	Jump To User Patch 1
066H	Configure Advanced Cache Registers
068H	Enable External And CPU Caches
069H	Initialize System Memory (SMM)
06AH	Display Cache Size
06CH	Display Shadow Messages

Post Code	Checkpoint Description
06EH	Display Non-Disposable Segments
070H	Display Error Messages
072H	Check For Configuration Errors
076H	Test Keyboard
07CH	Set Up Hardware Interrupt Vectors
07EH	Test CoProcessor
080H	Disable OnBoard I/O Ports
081H	Initialize PNP Devices (Late)
082H	Detect And Install RS232 Ports
083H	Configure IDE Controller
084H	Detect And Install External Parallel Port(s)
085H	Configure ISA PNP Devices
086H	Re-Initialize OnBoard I/O Ports
087H	Configure PNP Devices On Motherboard (MCD)
088H	Initialize BIOS Data Area (BDA)
089H	Enable Non-Maskable Interrupt
08AH	Initialize Extended BIOS Data Area (EBDA)
08BH	Initialize Mouse
08CH	Initialize Floppy Diskette
08FH	Initialize Multi-Boot Table(s)
090H	Initialize Fixed Disk(s)
091H	Set Fast IDE Timings
092H	Jump To User Patch #2
093H	Build MPTable For MultiProcessor Boards
095H	Install CDROM For Boot
096H	postDoShutdown8
098H	Search For Option ROMs
09CH	Initialize Power Management
09DH	Initialize System Security
09EH	Enable Hardware Interrupts
09FH	Record Number Of Fixed Disks Installed
0A0H	Set Time Of Day
0A4H	Initialize Key Repeat Rate
0A8H	Erase “F2” Prompt
0AAH	Scan For “F2” Key Entered
0ACH	Enter Setup (If Directed To Do So)
0AEH	Clear Flag Indicating That System Is “In POST”
0B0H	Check For Reported System Errors
0B2H	Post Done, Prepare To Boot Operating System
0B4H	Issue One Beep
0B5H	End Of Quiet Boot
0B6H	Check For Password (If Security Is Installed)

Post Code	Checkpoint Description
0B7H	Configure ACPI
0B9H	Prepare To Boot
0BCH	Clear Parity Checker
0BEH	Clear Screen (Optional)
0BFH	Check Virus And Backup Reminders
0C0H	Try To Boot Operating System With Int19
0C1H	Initialize Phoenix Error Manager
0C2H	Log System Errors
0C3H	Display System Errors
0C6H	Initialize Notebook Docking (Early)
0C7H	Initialize Notebook Docking (Late)
0C9H	Execute Extended BIOS Checksumming

Support Software

The following updates can be provided through the Rugged Mobile Computing service center.

BIOS Update Disk	Phoenix Flash BIOS update disk containing PHLASH.EXE, the System BIOS image for the FBD, and support files. This disk only updates the BIOS extensions contained in main block #3, the System BIOS contained in main block #4, and both parameter blocks.
Boot Block Update Disk	Phoenix Flash BIOS update disk containing PHLASH.EXE, the System BIOS image for the FBD, and support files. This disk only updates the boot block.

The RMC must be opened to reflash the boot block or system BIOS; thus, violating the warranty if accomplished by the user. All BIOS upgrades must be accomplished by Raytheon Service Personnel.

Hardware Support

System Compatibility Overview

The RMC products are designed to be compatible with operating systems from Microsoft, including Windows 95, Windows 98, Windows NT 4.0 and Windows 2000.

System Memory Map

After the BIOS POST has been completed, the physical addresses from the CPU are mapped into memory according to the following table. Regions that are routed to PCIbus will get routed to the DIU ISA interface (if attached) if no PCI device claims the transaction. All shadowed BIOSes are write protected by the BIOS.

Some devices that may claim PCIbus memory space are listed in this section. The system BIOS and/or operating system drivers dynamically allocate these devices.

Table 5. RMC Memory Map

Range	CPU address	Region	Cached
0 to 640K	00000000- 0009FFFF	DRAM	yes
640K to 768K	000A0000- 000BFFFF	VGA memory window	no
768K to 800K	000C0000- 000CBFFF	Shadowed VGA BIOS (48K)	yes
800K to 912K	000CC000- 000E3FFF	Available for PCI or DIU ISA cards, or shadowed BIOS extensions	no yes
912K to 1M	000E4000- 000FFFFF	Shadowed System BIOS	yes
1M to Top of Memory	00100000-	DRAM If no DRAM, PCI or DIU ISA	yes no
	base + 0 - 1000	82558 Ethernet controller	no
		CPU board SCSI controller	no
		DIU board SCSI controller	no
		CardBus memory windows	no
		VGA Frame buffer/BitBLT	no
Top of Memory to (4.0G – 512K)	- FFF7FFFF	Available for PCI or DU ISA add-in cards.	no
Top 512K	FFF80000- FFFFFFFF	Flash boot Device(BIOS)	no

I/O Map

The following registers are accessible in the I/O space. Some compatibility aliasing of PC compatibility registers exists as well, which is not listed here.

All accesses listed are positively decoded. If the unit is docked, any address not listed here will be subtractivly decoded by the 380FB Docking Bridge and forwarded to the DIU PCIbus. Any access not claimed by a PCIbus device on the DIU PCIbus will be forwarded to the DIU ISAbus. If the unit is not docked, a PCIbus master-abort will occur, returning undefined data to the CPU.

The addresses 0x0279 and 0x0A79 are reserved for ISA Plug and Play compatibility.

Table 6. RMC I/O Map

Port Address	Functional group	R/W	Usage
0000	DMA Controller 1	R/W	DMA 1 Channel 0 address
0001		R/W	DMA 1 Channel 0 count
0002		R/W	DMA 1 Channel 1 address
0003		R/W	DMA 1 Channel 1 count
0004		R/W	DMA 1 Channel 2 address
0005		R/W	DMA 1 Channel 2 count
0006		R/W	DMA 1 Channel 3 address
0007		R/W	DMA 1 Channel 3 count
0008		R W	DMA 1 Command DMA 1 Status
0009		W	DMA 1 Write Request
000A		W	DMA 1 Single Mask Bit
000B		W	DMA 1 Write Mode
000C		W	DMA 1 Clear byte pointer
000D		W	DMA 1 Master clear
000E		W	DMA 1 Clear Mask
000F		R/W	DMA 1 Read/write all mask register bits
0020	Interrupt Controller 1	R/W	INT 1 Control
0021		R/W	INT 1 Mask
0022	PM2_CTL	R/W	ACPI Pwr Control 2
0040	Timer/Counter	R/W	Counter 0 Count/Status
0041		R/W	Counter 1 Count/Status
0042		R/W	Counter 2 Count/Status
0043		W	Command Mode
0060	Keyboard Controller	R/W R	Data I/O register Reset Xbus IRQ12/M and IRQ1
0061	NMI Status and Control	R W	NMI Status NMI Control

Port Address	Functional group	R/W	Usage	
0064	Keyboard Controller	R W	Status Register Command Register	
0070	Real-time clock, NMI	W	RTC Index Register = bits 6-0 NMI Enable = bit 7	
0071		R/W	RTC Data Register	
			0	seconds
			1	seconds alarm
			2	minutes
			3	minutes alarm
			4	hours
			5	hours alarm
			6	day of week
			7	date of month
			8	month
			9	year
			A	status A
			B	status B
			C	status C
			D	status D
			E … FF	NVRAM
0080	DMA Controller 1	R/W	DMA Page (reserved)	
0081		R/W	DMA Channel 2 page register	
0082		R/W	DMA Channel 3 page register	
0083		R/W	DMA Channel 1 page register	
0084		R/W	DMA Page (reserved)	
0085		R/W	DMA Page (reserved)	
0086		R/W	DMA Page (reserved)	
0087		R/W	DMA Channel 0 page register	
0088	DMA Controller 2	R/W	DMA Page (reserved)	
0089		R/W	DMA Channel 6 page register	
008A		R/W	DMA Channel 7 page register	
008B		R/W	DMA Channel 5 page register	
008C		R/W	DMA Page (reserved)	
008D		R/W	DMA Page (reserved)	
008E		R/W	DMA Page (reserved)	
008F		R/W	DMA Low Page Register Refresh	
0092	Port 92	R/W	Port 92	
00A0	Interrupt Controller 2	R/W	INT 2 Control	
00A1		R/W	INT 2 Mask	
00B2	Advanced Power Management	R/W	Control	
00B3		R/W	Status	
00C0	DMA Controller 2	R/W	DMA 2 Channel 4 address	

Port Address	Functional group	R/W	Usage
00C2		R/W	DMA 2 Channel 4 count
00C4		R/W	DMA 2 Channel 5 address
00C6		R/W	DMA 2 Channel 5 count
00C8		R/W	DMA 2 Channel 6 address
00CA		R/W	DMA 2 Channel 6 count
00CC		R/W	DMA 2 Channel 7 address
00CE		R/W	DMA 2 Channel 7 count
00D0		R W	DMA 2 Status DMA 2 Command
00D2		W	DMA 2 Write Request
00D4		W	DMA 2 Write Single Mask Bit
00D6		W	DMA 2 Write Mode
00D8		W	DMA 2 Clear Byte Pointer
00DA		W	DMA 2 Master Clear
00DC		W	DMA 2 Clear Mask
00DE		R/W	DMA 2 Read/Write all register mask bits
00F0	Coprocessor	W	Coprocessor Error
015C	SuperI/O	R/W	Index Register
015D	Configuration	R/W	Data Register
0170	Secondary IDE	R/W	Data
0171		R/W	Error/Features
0172		R/W	Sector Count
0173		R/W	Sector Number
0174		R/W	Cylinder Low
0175		R/W	Cylinder High
0176		R/W	Drive/Head
0177		R/W	Status/Command
x180 – x1EF	unused	R/W	
01F0	Primary IDE	R/W	Data
01F1		R/W	Error/Features
01F2		R/W	Sector Count
01F3		R/W	Sector Number
01F4		R/W	Cylinder Low
01F5		R/W	Cylinder High
01F6		R/W	Drive/Head
01F7		R/W	Status/Command
0220-0223	Sound Generator	R/W	20-voice FM Synthesizer address and data registers
0224		R/W	Mixer address register
0225		R/W	Mixer data register

Port Address	Functional group	R/W	Usage
0226		R W	Power management status Reset
0227		R/W	Power management register
0228-0229		R/W	11-voice FM synthesizer address and data registers
022A		R	Input buffer data
022C		R W	Output buffer status register Output buffer data
022E		R	Write buffer status
022F		R/W	Extended mode FIFO address
0278	Parallel Port (Alternate decode)	R/W	Data register
0279		R	Status register
027A		R/W	Control register
027B			Reserved
02E8	COM4 Serial Port (Alternate decode for RS-232 port)	R W	Receiver buffer Transmitter buffer
02E9		R/W	Baud rate divisor latch (LSB)
		R/W	Interrupt enable register
02EA		R/W	Baud rate divisor latch (MSB)
02EB		R W	Interrupt ID register FIFO Control register
02EC		R/W	Line control register
02ED		R/W	Modem control register
02EE		R	Line status register
02EF		R	Modem status register
02F8	COM2 Serial Port	R/W	Scratch Pad
02F9		R W	Receiver buffer Transmitter buffer
02FA		R/W	Baud rate divisor latch (LSB)
02FB		R/W	Interrupt enable register
02FC		R/W	Baud rate divisor latch (MSB)
02FD		R W	Interrupt ID register FIFO Control register
02FE		R/W	Line control register
02FF		R/W	Modem control register
0374	Secondary IDE	R	Line status register
0375		R	Modem status register
0376		R/W	Scratch Pad
			Reserved
			Reserved
			Alt Status/Device control

Port Address	Functional group	R/W	Usage
0378	Parallel Port	R/W	Data register
0379		R	Status register
037A		R/W	Control register
037B			Reserved
0388-038B	Sound Generator	R/W	20-voice FM Synthesizer (same as x220-x223)
03B4	VGA Controller	R/W	CRT Controller index (mono)
03B5		R/W	CRT Controller data (mono)
03BA		R W	Input Status Register 1 (mono) Feature control output (mono)
03BC	Parallel Port (Alternate location)	R/W	Data register
03BD		R	Status register
03BE		R/W	Control register
03BF			Reserved
03C0	VGA Controller	W	Attribute controller Index/Data
03C1		R	Attribute controller Index/Data
03C2		R W	Input Status Register 0 Miscellaneous output
03C4		R/W	Sequencer Index
03C5		R/W	Sequencer Data
03C6		R/W R/W	Video DAC pixel mask Hidden DAC register
03C7		R W	DAC State Pixel address read mode
03C8		R/W	Pixel mask write mode
03C9		R/W	Pixel data
03CA		R	Feature control read-back
03CC		R	Miscellaneous output read back
03CE		R/W	Graphics controller index
03CF		R/W	Graphics controller data
03D0		R/W	Flat Panel Extensions Index
03D1		R/W	Flat Panel Extensions data
03D2		R/W	Multimedia Extensions Index
03D3		R/W	Multimedia Extensions data
03D4		R/W	CRT controller index (color)
03D5		R/W	CRT controller data (color)
03D6		R/W	Configuration Extensions Index
03D7		R/W	Configuration Extensions Data
03DA		R W	Input Status Register 1 (color) Feature Control (color)

Port Address	Functional group	R/W	Usage
03E8	COM3 Serial Port (Alternate decode for RS232 port)	R W	Receiver buffer Transmitter buffer
		R/W	Baud rate divisor latch (LSB)
03E9		R/W	Interrupt enable register
		R/W	Baud rate divisor latch (MSB)
03EA		R W	Interrupt ID register FIFO Control register
03EB		R/W	Line control register
03EC		R/W	Modem control register
03ED		R	Line status register
03EE		R	Modem status register
03EF		R/W	Scratch Pad
03F0	Floppy Disk Controller	R	Status Register A
03F1		R	Status Register B
03F2		R/W	Digital Output Register
03F3		R/W	Tape Driver Register
03F4		R W	Main Status Register Data Rate Select Register
03F5		R/W	Data Register
03F6	Primary IDE	R/W	Alt Status/Device control
03F7		R W	Digital Input Register Configuration Control Register
03F8	COM1 Serial Port	R W	Receiver buffer Transmitter buffer
		R/W	Baud rate divisor latch (LSB)
03F9		R/W	Interrupt enable register
		R/W	Baud rate divisor latch (MSB)
03FA		R W	Interrupt ID register FIFO Control register
03FB		R/W	Line control register
03FC		R/W	Modem control register
03FD		R	Line status register
03FE		R	Modem status register
03FF		R/W	Scratch Pad
04D0	Interrupt Controller 1	R/W	INTC-1Edge/Level Control
04D1	Interrupt Controller 2	R/W	INTC-2Edge/Level Control
0678	Parallel ECP Port (if Parallel Port at 278)	R/W R	Parallel Port/ECP/TEST FIFO Configuration Register A
0679		R	Configuration Register B
067A		R/W	Extended Control Register

Port Address	Functional group	R/W	Usage
0778	Parallel ECP Port (if Parallel Port at 378)	R/W R	Parallel Port/ECP/TEST FIFO Configuration Register A
0779		R	Configuration Register B
077A		R/W	Extended Control Register
07BC	Parallel ECP Port (if Parallel Port at 3BC)	R/W R	Parallel Port/ECP/TEST FIFO Configuration Register A
07BD		R	Configuration Register B
07BE		R/W	Extended Control Register
0CF8 – 0CFB (Dword only)	PCI Configuration	R/W	Configuration Address Register
0CFC – 0CFF		R/W	Configuration Data Register

The following devices will claim some PCIbus I/O space, but the system BIOS and/or operating system drivers dynamically allocate their base addresses.

Table 7. RMC Dynamically Configured I/O Map

Port Address	Functional group	R/W	Usage
USBA + 0-13h	USB Host/Controller	R/W	
BMIBA+ 0-Fh	PCI BusMstr IDE Ctlr	R/W	
PMBA+ 0-37h	Pwr Mgmt Registers	R/W	
SMBBA+0-Dh	SMbus Ctlr Registers	R/W	
base + 0 - 20h	Ethernet Controller	R/W	CSR Registers
?base16 + 0 - 1	Int CardBus controller	R/W	16bit legacy mode emulation
base + 0 - 20h and 800-844h	Int CardBus controller	R/W	CardBus socket registers ExCA Registers
base16 + 0 - 1	Ext CardBus controller	R/W	16bit legacy mode emulation
?	Ext CardBus controller	?	?
base + 0 - 20h and 800-844h	Ext CardBus controller	R/W	CardBus socket registers ExCA Registers
base + 0 - 7Fh	CPU SCSI controller	R/W	
base + 0 - 7Fh	DIU SCSI controller	R/W	**Subtractively Decoded!**

Interrupt Assignments

The following table lists the signals that are connected to the 82C59 compatible Interrupt Controllers. An 'X' denotes a hardware default/typical DOS-compatible allocation. An 'x' denotes other possible connections under software control (i.e. CMOS Configuration, PnP, ACPI, etc). IRQs not allocated to a device are available for add-in cards on the DIU ISAbus (if docked).

Under some operating systems/drivers, the Serial port interrupts can be shared. Windows 9x does support this, while Windows NT 4.0 does not. Also, PCI interrupts should be able to be routed to the same IRQ, forcing the drivers to chain their interrupt handlers. All other interrupt sources cannot share interrupts with other devices.

Table 8. PFS-098 IRQ Map

	IRQ0	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5	IRQ6	IRQ7	IRQ8	IRQ9	IRQ10	IRQ11	IRQ12	IRQ13	IRQ14	IRQ15	NMI
Timer	X																
Keyboard Controller		X															
PS/2 Mouse													X				
Cascade interrupt input			X														
RS232 Serial		x		x	X	x	x	x					x				
RS422/485 Serial		x		X	x	x	x	x					x				
Sound generator						x		x		x		x	x			x	
Floppy Disk		x		x	x	x	X	x					x				
LPT1		x		x	x	x	x	X					x				
Real time clock									X								
Numeric Coprocessor														X			
Primary EIDE															X		
Secondary EIDE																x	
Memory Parity/ECC Error (Disabled)																	X
CardBus Events (via SIRQ)		x		x	x	x	x	x		x	x	x	x		x	x	x
ACPI SCI Events										X							
PIRQA (input to PIIX4E)				x	x	x	x	x		x	x	x	x		x	x	
PIRQB (input to PIIX4E)				x	x	x	x	x		x	x	x	x		x	x	
PIRQC (input to PIIX4E)				x	x	x	x	x		x	x	x	x		x	x	
PIRQD (input to PIIX4E)				x	x	x	x	x		x	x	x	x		x	x	
Docking Station ISA Slots				x	x	x	x	x		x	x	x	x		x	x	x

The following table shows physical connections for PCI Interrupts in the system. The PCI slots have all 4 INTs connected, but single function PCI cards (most cards) will only use INTA (capitalized). For these add-in slots, letters indicate the PCIbus defined INT pins.

Table 9. RMC PCI/PIIX INT# Map

PIIX Interrupt Signal →	INTA	INTB	INTC	INTD
PIIX4E/USB Controller				X
Internal CardBus Controller			X	
External CardBus Controller			X	
CPU board SCSI Controller	X			
82558 Ethernet controller		X		
CPU PCI slot	d	A	b	c
DIU board SCSI Controller	X			
DIU PCI slot 1	A	B	c	d
DIU PCI slot 2	c	d	A	B

DMA Channels

The following table lists connections to the 82C37 compatible DMA controllers.

Table 10. RMC DMA Map

	8-bit DMA				16-bit DMA			
	DMA0	DMA1	DMA2	DMA3	DMA4	DMA5	DMA6	DMA7
IEE1284 ECP	X	X		X				
Floppy Disk Ctrlr		X		X				
Audio			X					
DMA0-3 Cascade					X			

Unassigned or unused DMA channels are available for add-in cards on the DIU ISAbus or the CardBus controllers.

CPU/Chipset

The RMC use the Intel MMC2 Pentium-II module and an Intel 82371EB (PIIX4E) ISA/IDE Xcelerator to form the PC/AT compatible CPU/Chipset pair.

Intel MMC2 Mobile Module with 233Mhz Pentium-II Processor

The RMC CPU board uses a Pentium® II Mobile Module CPU in a 400-pin BGA package at either 233Mhz, 266Mhz, or 333Mhz core frequency. The Pentium® II processor on-board includes a 32KB L1 code and data cache. This module itself includes a 512K direct-mapped L2 cache, which can cache up to 256MB of system memory when using 16Mbit DRAMs (up to 512MB of system memory when using 64Mbit DRAMs).

All CPU and PCI clocks are generated by a PLL clock synthesizer. The Pentium® II bus clock frequency is set at 66.66 MHz. The resulting CPU core frequency is 233 MHz.

Table 11. PCI Clock Frequency

Pentium®II Frequency	Processor Bus Frequency,	PCI Clock Frequency[1]
233MHz	66MHz	33MHz
266MHz	66MHz	33MHz
333MHz	66MHz	33MHz

[1]66MHz CPU bus is actually 66.66MHz, hence 33MHz PCI bus is actually 33.33MHz.

The MMC2 module supports an AGP bus interface for high performance video controllers. The RMC CPU board will not use this port.

DRAM

The computer supports CPU-to-memory and PCI-to memory cycles, as well as CPU-to-PCI cycles.

CPU memory is installed in two 144 pin 3.3V gold-plated SO DIMM sockets on the CPU board. EDO, SDRAM, or ECC SDRAM modules may be used. EDO Parity is not supported. Single or double sided, symmetrical or asymmetrical, 60ns EDO DRAM or 66Mhz SDRAM memory may be used. (Note that the 66Mhz SDRAM limitation is a function of the CPU speed.) The following sizes may be used (as available):

- 1Mx64 (8MB)
- 2Mx64 (16MB)
- 4Mx64 (32MB)
- 8Mx64 (64MB)
- 16Mx64 - (128MB)

Either or both SO DIMM sockets may be populated. Each socket may have a different size of memory module. Different technologies of modules (EDO and SDRAM) CANNOT be mixed.

JEDEC has standardized a Serial Presence detect mechanism for SO DIMMs utilizing an I^2C interface to read back information about depth, width, number of banks, addressing, error checking schemes (e.g. ECC or Parity), and other pertinent information for configuring the memory controller. The Chameleon is set up to be able to read this configuration with its SMbus interface.

Connectors

DC Power Input connector (Chameleon, Gecko)

The DC Power Input connector receives raw DC from either the DIU or the AC Adapter. This connector is Molex part number 26-60-4030 or form, fit and function equivalent.

Table 12. DC Power Input Connector

Pin	Signal
Pin 1	DC-IN +
Pin 2	DC-IN -
Pin 3	n/c

DC Power Input connector (Iguana)

The Iguana DC Power Input connector receives raw DC from a military connector. This connector is MS27473E14F5S or form, fit and function equivalent. Reference Raytheon Part Number 3195295-13.

Table 13. Iguana Power Input Connector

Pin	Signal
Pin A,B,C	n/c
Pin D	DC-IN +
Pin E	DC-IN -

External 8-bit SCSI-3 connector

The SCSI connector is a .050, 50 conductor mini D sub. The Vendor Part Number is: AMP 787395-5 or a form, fit and function equivalent.

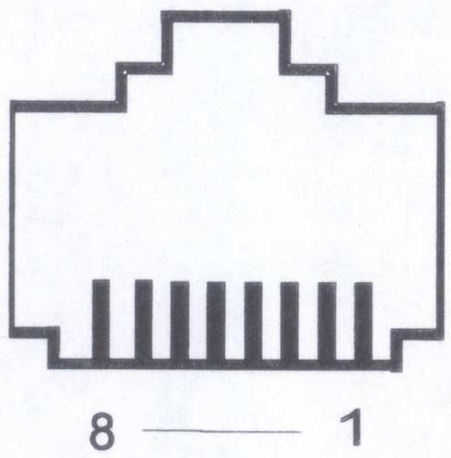
Table 14. RMC SCSI connector

Pin	Description	Pin	Description
1	Signal GND	2	~DB0
3	Signal GND	4	~DB1
5	Signal GND	6	~DB2
7	Signal GND	8	~DB3
9	Signal GND	10	~DB4
11	Signal GND	12	~DB5
13	Signal GND	14	~DB6
15	Signal GND	16	~DB7
17	Signal GND	18	~DBP
19	Signal GND	20	Signal GND
21	Signal GND	22	Signal GND
23	Signal GND	24	Signal GND
25	NC	26	Terminator Power
27	Signal GND	28	Signal GND
29	Signal GND	30	Signal GND
31	Signal GND	32	~ATN
33	Signal GND	34	Signal GND
35	Signal GND	36	~BSY
37	Signal GND	38	~ACK
39	Signal GND	40	~RST
41	Signal GND	42	~MSG
43	Signal GND	44	~SEL
45	Signal GND	46	~C/D
47	Signal GND	48	~REQ
49	Signal GND	50	~I/O

Ethernet connector

The 10/100 Base-T port uses a RJ45 connector with the following pin-out. This connector is an AMP 555164-1 or a form, fit and function equivalent. The pins noted as AC-term are connected through 75 ohms to a common net, which is AC coupled to ground.

Table 15. Ethernet Connector



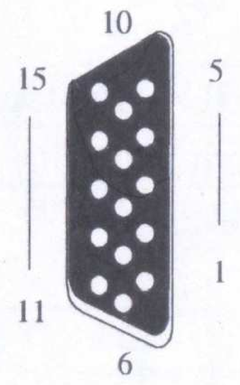
Pin	Signal
1	Transmit +
2	Transmit -
3	Receive +
4	AC-term
5	AC-term
6	Receive-
7	AC-term
8	AC-term

VGA Connector

The VGA DB-15 is a sealed female connector (Positronics ODD15F4C70T20-792.39) which connects to a standard CRT monitor connector.

Table 16. VGA DB-15 Connector Pins

Pin	Signal	Pin	Signal
1	Red	9	(key)
2	Green	10	Ground
3	Blue	11	n/c
4	n/c	12	DDC Data
5	Ground	13	Horizontal sync
6	Ground	14	Vertical sync
7	Ground	15	DDC Clk
8	Ground		

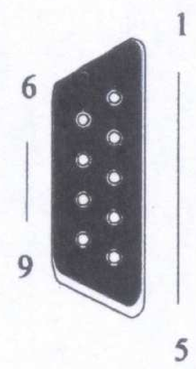


RS-232 Connector

The RS232 serial port is a sealed male DB-9 DTE connector, Positronics part number MD9M5C70T20-792.38. The pin-out of this connector follows the RS-232-E standard.

Table 17. COM-A DB-9 Connector Pins

Pin	Signal	Pin	Signal
1	Carrier detect	6	Data set ready
2	Receive data	7	Request to send
3	Transmit data	8	Clear to send
4	Data terminal ready	9	Ring indicator
5	Signal ground		

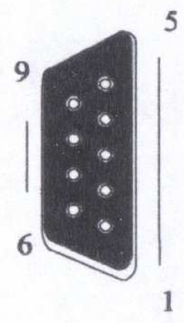


RS422/485 Connector

The RS422/485 serial port is a sealed female DB-9 DTE connector, Positronics part number MD9F5C70T20-792.38. Note that there is no industry standard pin-out for RS422 or RS485.

Table 18. COM-B DB-9 Connector Pins

Pin	Signal	Pin	Signal
1	Signal Ground	6	Request to send +
2	Clear to send +	7	Request to send -
3	Clear to send -	8	Transmit data + (output)
4	Receive Data - (in)	9	Transmit data - (output)
5	Receive Data + (in)		

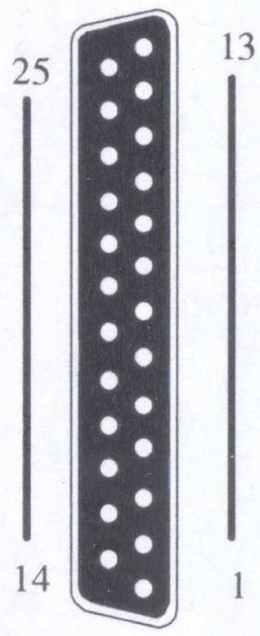


Parallel Port Connector

The parallel port is a sealed female IEEE1284-A 25 pin Dsub connector Positronics part number MD25F5C70T20-792.38. This connector pin-out follows the IEEE-1284-A specification.

Table 19. LPT1 Connector Pins

Parallel Port Connector (Internal)			
Pin	**Signal**	**Pin**	**Signal**
1	~Strobe	14	~AF Auto Feed
2	D0	15	~ERR
3	D1	16	~INIT
4	D2	17	~SELIN
5	D3	18	Signal GND
6	D4	19	Signal GND
7	D5	20	Signal GND
8	D6	21	Signal GND
9	D7	22	Signal GND
10	~ACK	23	Signal GND
11	BUSY	24	Signal GND
12	PE (Paper End)	25	Signal GND
13	SELECT		



External PS/2 Keyboard/Mouse connector

The external keyboard and mouse connector allows an external PS/2 keyboard or PS/2 mouse to be attached. These signals can be run to a single Mini-DIN connector to allow a splitter cable to provide standard connectors for both a keyboard and a mouse connection. A 1.0A resetable fuse (Raychem) fuses the +5V power to the keyboard and the mouse.

The connector used is a female Molex 90136-2206 or form, fit and function equivalent 0.100" right-angle shrouded connector.

Table 20. External PS/2 Keyboard/Mouse Connector

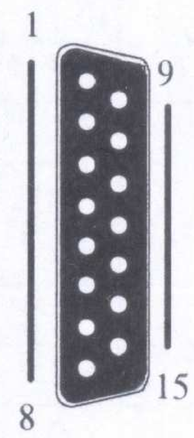
Pin	Signal
1	Mouse Data
2	Kbd Data
3	GND
4	+5V
5	Mouse Clock
6	Kbd Clock

Multimedia Connector

The Multimedia connector allows external connection for a mono microphone, line-in and line-out devices, as well as one USB port. This connector does not follow any industry standards, and as such a special cable can be provided to connect to most devices. The connector is a sealed female DB15 connector Positronics part number MD15F5C70T20-792.38.

Table 21. Multimedia Connector

Pin	Signal	Pin	Signal
1	AGND	9	Mic In
2	AGND	10	Line In L
3	Line In R	11	AGND
4	Line Out L	12	Line Out R
5	AGND	13	DGND
6	USB +5V	14	USB-
7	DGND	15	USB+
8	DGND		



Docking Signal connector

The Docking Signal connector provides the connections for all signals between the CPU board and the DIU board. Power connections are made on a separate connector. This connector is a Molex 52943-1200.

Table 22. DIU Docking Connector

Pin	Signal	Pin	Signal
1*	GND	31*	GND
2*	AD0	32*	AD1
3	AD2	33	AD3
4	AD4	34	AD5
5	GND	35	GND
6	AD6	36	AD7
7	AD8	37	AD9
8	AD10	38	AD11
9	GND	39	GND
10	AD12	40	AD13
11	AD14	41	AD15
12	PAR	42	SERR#
13	GND	43	GND
14	PERR#	44	STOP#
15	DEVSEL#	45	TRDY#
16	IRDY#	46	FRAME#
17	GND	47	GND
18	AD16	48	AD17
19	AD18	49	AD19
20	AD20	50	AD21
21	GND	51	GND
22	AD22	52	AD23
23	AD24	53	AD25
24	AD26	54	AD27
25	GND	55	GND
26	AD28	56	AD29
27	AD30	57	AD31
28	~REQ	58	~GNT
29*	GND	59*	GND
30*	CD2	60*	GND

Pin	Signal	Pin	Signal
61	CD1	91	GND
62	DCIN-	92	DCIN+
63	DCIN-	93	DCIN+
64	~PCILock	94	~dPwrGood
65	~Recovery	95	~UndckGnt
66	GND	96	GND
67	PwrGood	97	~DockIntr
68	~QEN0	98	~QPCIEN
69	~SUSB	99	~WAKE
70	GND	100	GND
71	C/~BE0	101	C/~BE1
72	C/~BE2	102	C/~BE3
73	PCPCIReq	103	PCPCIGnt
74	GND	104	GND
75	IDSEL	105	PCI_RST
76	PCI INTA	106	PCI INTB
77	PCI INTC	107	PCI INTD
78	GND	108	GND
79	IRQ4	109	IRQ3
80	IRQ6	110	IRQ5
81	IRQ9	111	IR7
82	GND	112	GND
83	IRQ11	113	IRQ10
84	IRQ14	114	IRQ12
85	IRQ15	115	IOCHK
86	GND	116	~ClkRun
87	PCI Clk	117	GND
88	GND	118	GND
89	DCIN-	119	DCIN+
90	DCIN-	120	DCIN+

Docking Power connector

The docking power connector provides raw DC power to the Chameleon. The DC power comes from the DIU power supply and is a Molex 26-60-4030 or a form, fit and function equivalent.

This connector may not be needed, pending investigation of use of the Docking Signal connector to provide this power to the CPU board.

Table 23. DC Power Connector

Pin	Signal
1	DC-IN +
2	DC-IN -
3	n/c

Internal Wide SCSI connector

A 16-bit Wide SCSI-3 "P" (Primary) connector on the DIU board uses a AMP 749069-7 or a form, fit and function equivalent connector. The pin-out for this connector implements a single-ended Wide SCSI-3 connection.

Table 24. Wide SCSI-3 Connector

Wide UltraSCSI-3 Connector			
Pin	**Signal**	**Pin**	**Signal**
1	GND	35	-DB(12)
2	GND	36	-DB(13)
3	GND	37	-DB(14)
4	GND	38	-DB(15)
5	GND	39	-DB(P1)
6	GND	40	-DB(0)
7	GND	41	-DB(1)
8	GND	42	-DB(2)
9	GND	43	-DB(3)
10	GND	44	-DB(4)
11	GND	45	-DB(5)
12	GND	46	-DB(6)
13	GND	47	-DB(7)
14	GND	48	-DB(P)
15	GND	49	GND
16	GND	50	GND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	RSRVD	53	RSRVD

Wide UltraSCSI-3 Connector			
Pin	**Signal**	**Pin**	**Signal**
20	GND	54	GND
21	GND	55	-ATN
22	GND	56	GND
23	GND	57	BSY
24	GND	58	-ACK
25	GND	59	-RST
26	GND	60	-MSG
27	GND	61	-SEL
28	GND	62	-C/D
29	GND	63	-REQ
30	GND	64	-I/O
31	GND	65	-DB(8)
32	GND	66	-DB(9)
33	GND	67	-DB(10)
34	GND	68	-DB(11)

ISAbus Connectors

Two ISAbus connectors are provided in the DIU. The connectors are AMP part number 176139-3 or a form, fit and function equivalent.

Table 25. PCIbus Connector

Pin	Signal Name	Pin	Signal Name
B1	GND	A1	IOCHK-
B2	RSTDRV	A2	SD7
B3	Vcc	A3	SD6
B4	IRQ9	A4	SD5
B5	-5 V	A5	SD4
B6	DRQ2	A6	SD3
B7	-12 V	A7	SD2
B8	0WS-	A8	SD1
B9	+12 V	A9	SD0
B10	GND	A10	IOCHRDY
B11	SMEMW-	A11	AEN
B12	SMEMR-	A12	SA19
B13	IOW-	A13	SA18
B14	IOR-	A14	SA17
B15	DACK3-	A15	SA16
B16	DRQ3	A16	SA15
B17	DACK1-	A17	SA14

Pin	Signal Name	Pin	Signal Name
B18	DRQ1	A18	SA13
B19	REFRESH-	A19	SA12
B20	SYSCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DACK2-	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	Vcc	A29	SA2
B30	OSC	A30	SA1
B31	GND	A31	SA0
KEY		KEY	
D1	MEMCS16-	C1	SBHE-
D2	IOCS16-	C2	LA23
D3	IRQ10	C3	LA22
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0-	C8	LA17
D9	DRQ0	C9	MEMR-
D10	DACK5-	C10	MEMW-
D11	DRQ5	C11	SD8
D12	DACK6-	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7-	C14	SD11
D15	DRQ7	C15	SD12
D16	Vcc	C16	SD13
D17	Master-	C17	SD14
D18	GND	C18	SD15

PCIbus Connectors

Two PCI standard 124-pin vertical card-edge receptacle connectors are provided on the DIU board. The connectors are AMP145154-4 or a form, fit and function equivalent.

Table 26. PCIbus Connector

	Component Side	Back Side
1	-12V	~TRST
2	TCK	+12V
3	GND	TMS
4	N/C	TDI
5	+5V	+5V
6	+5V	~INTA
7	~INTB	~INTC
8	~INTD	+5V
9	~PRSNT1	~CLKRUN (Reserved)
10	Reserved	+5V
11	~PRSNT2	Reserved
12	GND	GND
13	GND	GND
14	Reserved	Reserved
15	GND	~RST
16	CLK	+5V
17	GND	~GNT
18	~REQ	GND
19	+5V	Reserved
20	AD31	AD30
21	AD29	+3.3V
22	GND	AD28
23	AD27	AD26
24	AD25	GND
25	+3.3V	AD24
26	C/~BE3	IDSEL
27	AD23	+3.3V
28	GND	AD22
29	AD21	AD20
30	AD19	GND
31	+3.3V	AD18
32	AD17	AD16
33	C/~BE2	+3.3V
34	GND	~FRAME
35	~IRDY	GND
36	+3.3V	~TRDY
37	~DEVSEL	GND
38	GND	~STOP
39	~LOCK	+3.3V
40	~PERR	SDONE
41	+3.3V	~SBO
42	~SERR	GND
43	+3.3V	PAR
44	C/~BE1	AD15
45	AD14	+3.3V

	Component Side	Back Side
46	GND	AD13
47	AD12	AD11
48	AD10	GND
49	GND	AD09
50	KEY	
51	KEY	
52	AD08	C/~BE0
53	AD07	+3.3V
54	+3.3V	AD06
55	AD05	AD04
56	AD03	GND
57	GND	AD02
58	AD01	AD00
59	+5V	+5V
60	~ACK64 (pull up)	~REQ64 (pull up)
61	+5V	+5V
62	+5V	+5V

RMC Environmental and EMC Specifications

The RMC system is designed to meet the following environmental specifications:

Table 27. RMC Environmental Specifications

Temperature (Ambient)	Operating : -25°C to 50°C (-13°F to +122°F) Non-operating : -32°C-65°C (-25°F to +150°F)
Solar Loading	To internal temperature of +63°C (+145 °F)
Shock/Drop Test	Dropped from 18" height on all edges, faces/corners
Vibration	Non Operating: Frequency range: 5-55 Hz; 0.7 G at 5-15 Hz; 1.2 G at 16-25 Hz; 3G at 26-55 Hz
Altitude	Operating: 15,000ft Non-operating: 30,000ft
Rain Operating	1.8 inches per hour in 20 mph wind for 30 minutes
Humidity	Operating: 10-95% Non-operating: 5-95%
Sand/Dust	20 ± 3 mph for 30 minutes, dust concentration, 10.6 ± 0.7 g/m^3, sand concentration, 2.2 ± 0.5 g/m^3
EMI/EMC	Requirements of US Title 47, Code of Federal Regulations, Federal Communications Commission, Part 15, Industrial Use
Nuclear, Biological, and Chemical Warfare	Operable while the user is fully dressed in MOPP-IV Chemical Warfare (NBC) gear. Easily decontaminated, using standard methods, without degradation of performance or damaging the surface.
Fungus	Certified that materials used do not support fungal growth
Salt Fog	Certified that no signs of corrosion exist after being exposed to an aqueous salt atmosphere
Electrical	110/220 VAC at 47-400 Hz, 18-32 VDC
Physical	14.0" W 4.5" H 12.5" D 13.5 lbs. (without battery)

Technical Support

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